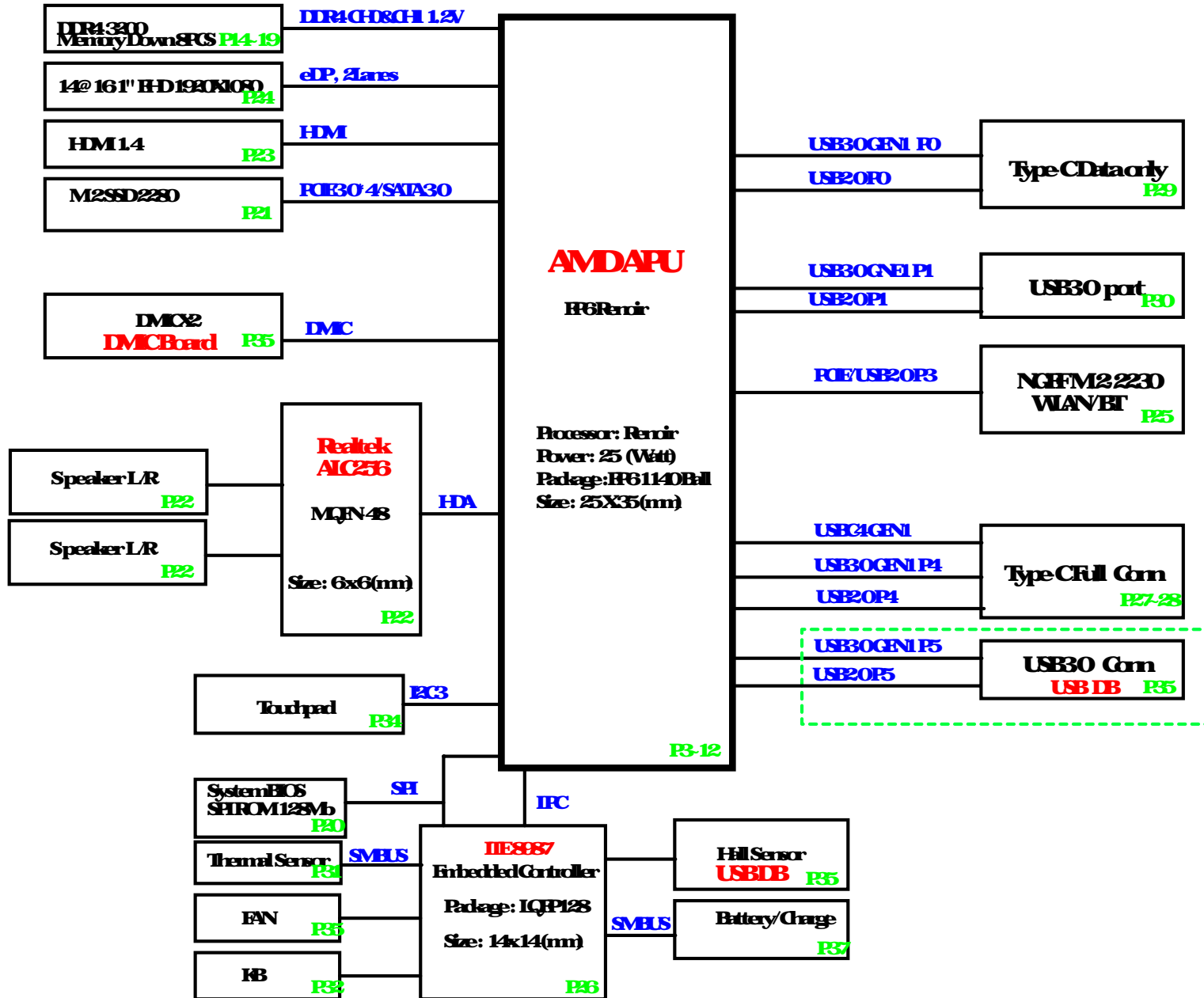
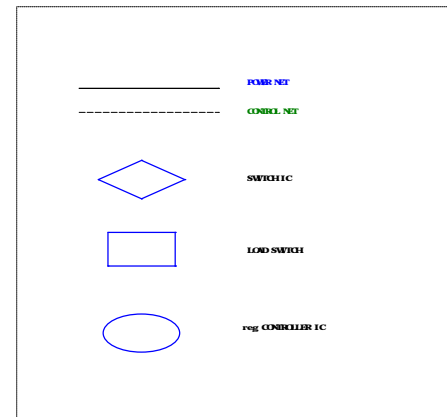
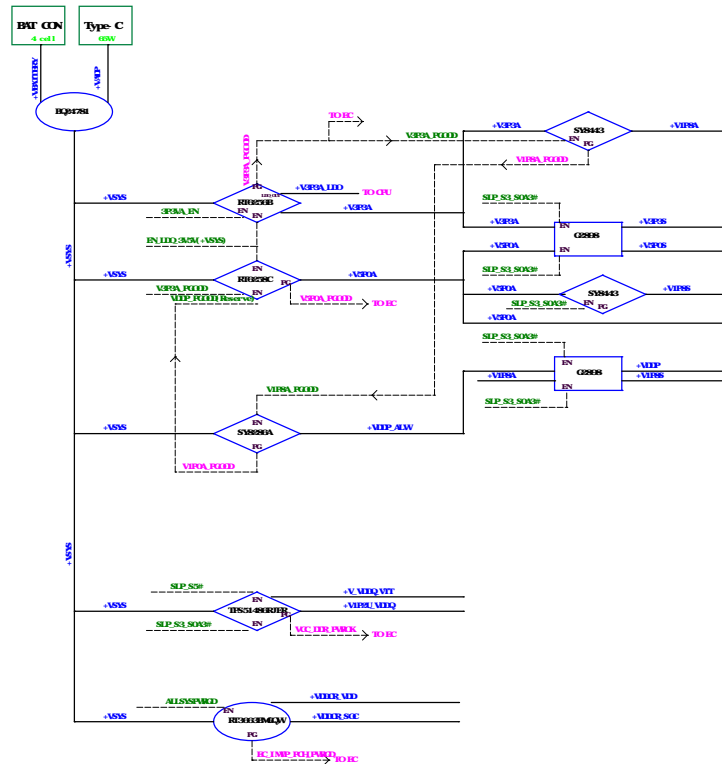


# NB2500 BLOCK DIAGRAM



**NB2500\_2501 V1 POWER MAP**



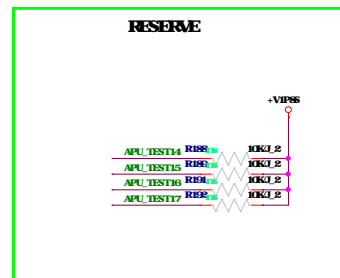
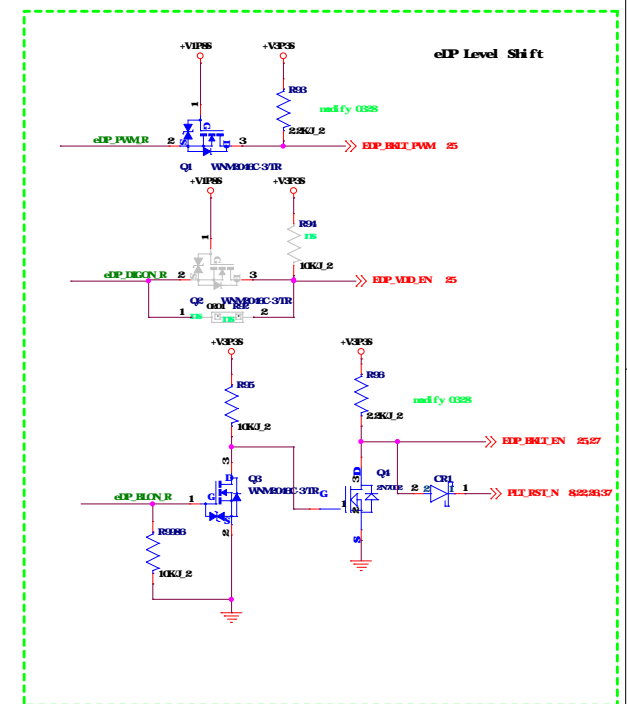
### Power On Sequence Diagram



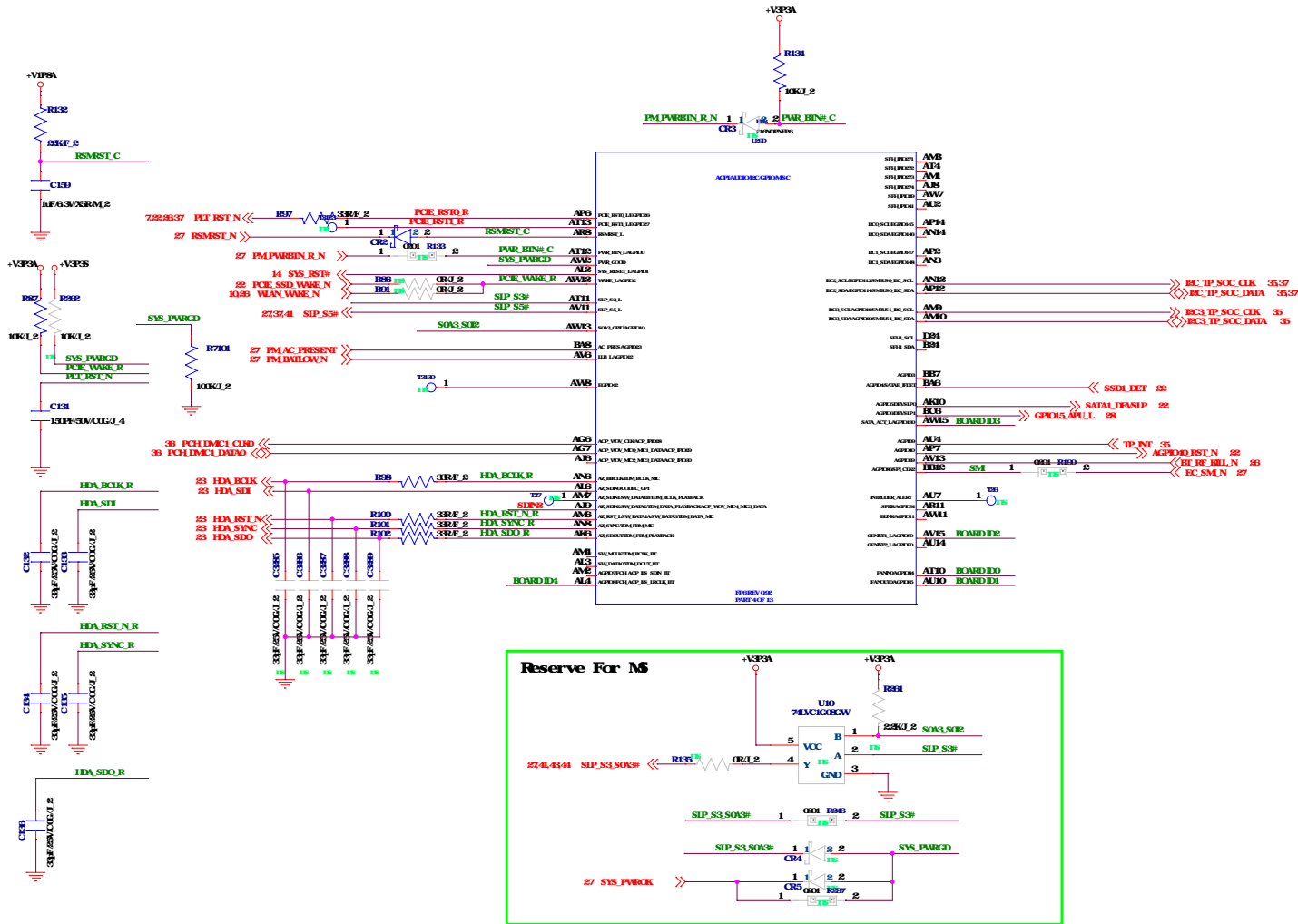




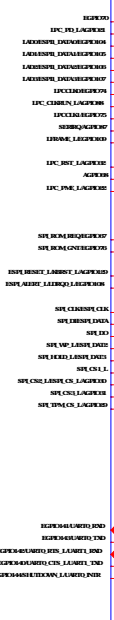
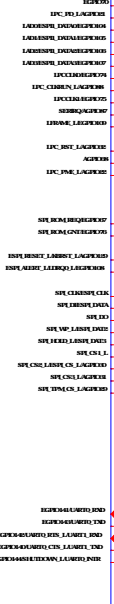
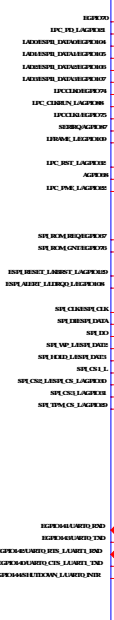




Boot VID Code		
SVC	SVD	Boot Voltage
0	0	1.1V
0	1	1.0V
1	0	0.9V
1	1	0.8V

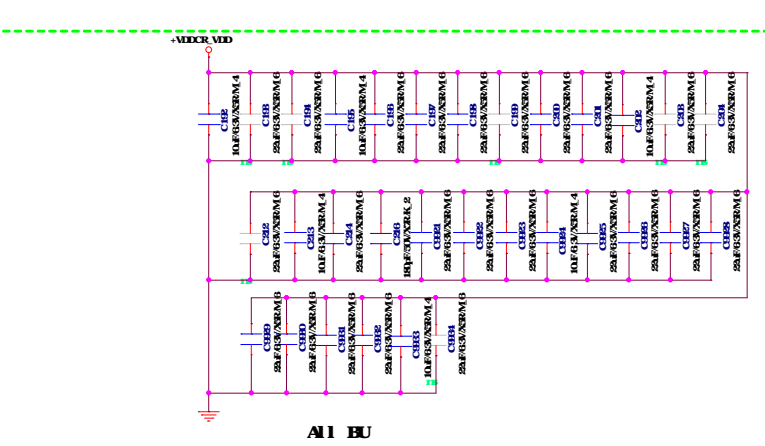




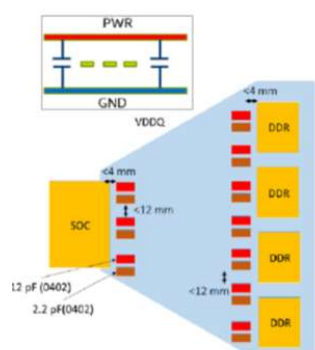
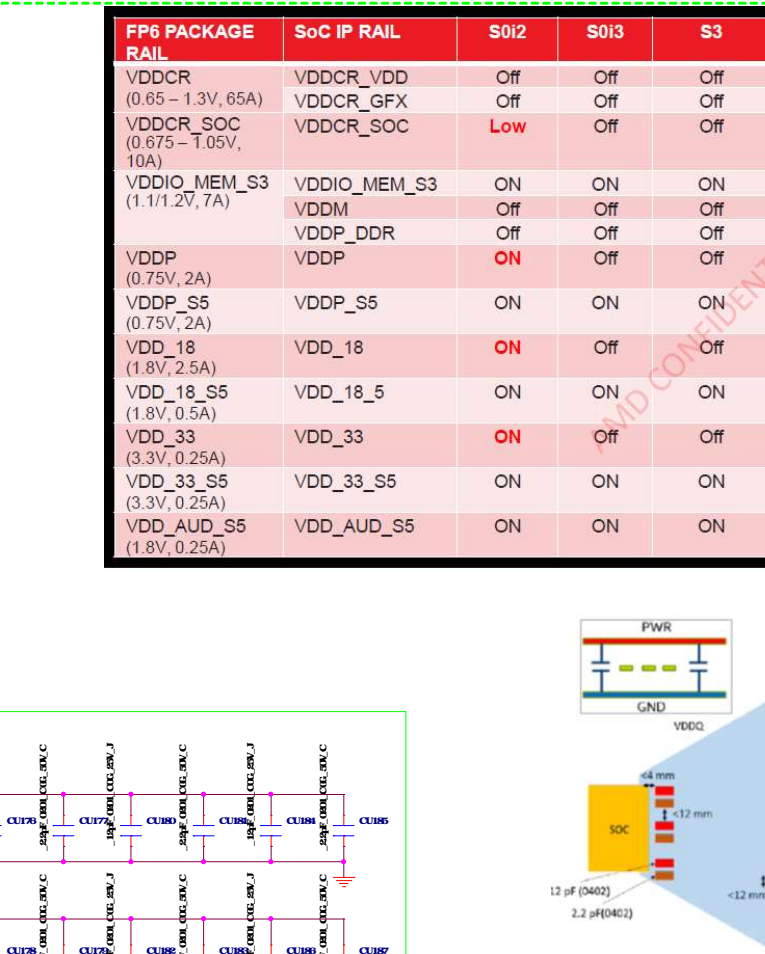




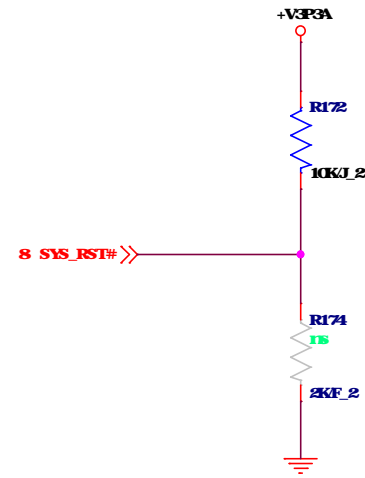
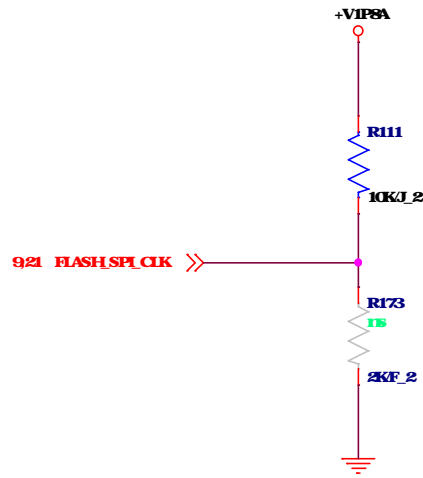




FP6 PACKAGE RAIL	SoC IP RAIL	S0i2	S0i3	S3
VDDCR (0.65 ~ 1.3V, 65A)	VDDCR_VDD	Off	Off	Off
	VDDCR_GFX	Off	Off	Off
VDDCR_SOC (0.675 ~ 1.05V, 10A)	VDDCR_SOC	Low	Off	Off
VDDIO_MEM_S3 (1.1/1.2V, 7A)	VDDIO_MEM_S3	ON	ON	ON
	VDDM	Off	Off	Off
	VDDP_DDR	Off	Off	Off
VDDP (0.75V, 2A)	VDDP	ON	Off	Off
VDDP_S5 (0.75V, 2A)	VDDP_S5	ON	ON	ON
VDD_18 (1.8V, 2.5A)	VDD_18	ON	Off	Off
VDD_18_S5 (1.8V, 0.5A)	VDD_18_5	ON	ON	ON
VDD_33 (3.3V, 0.25A)	VDD_33	ON	Off	Off
VDD_33_S5 (3.3V, 0.25A)	VDD_33_S5	ON	ON	ON
VDD_AUD_S5 (1.8V, 0.25A)	VDD_AUD_S5	ON	ON	ON

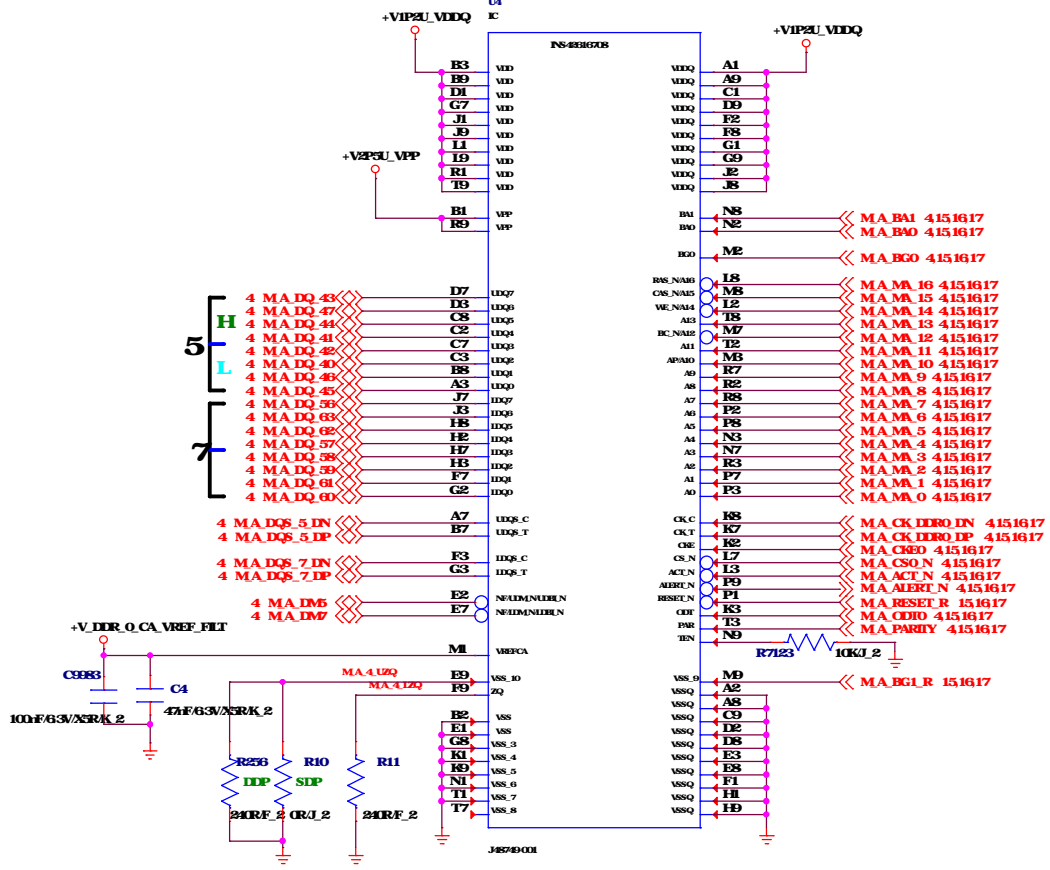






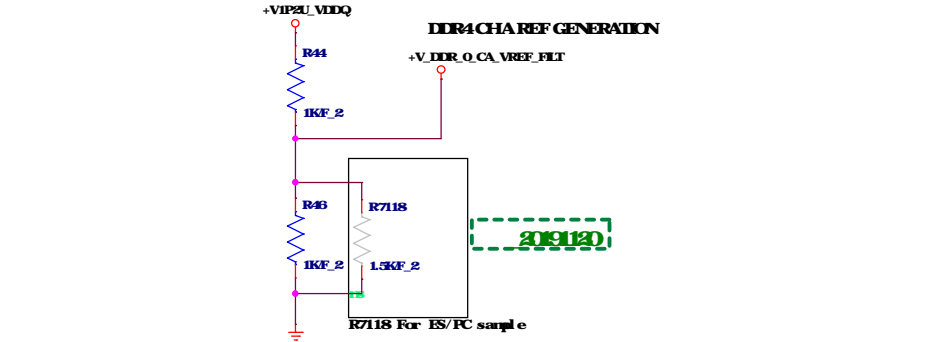
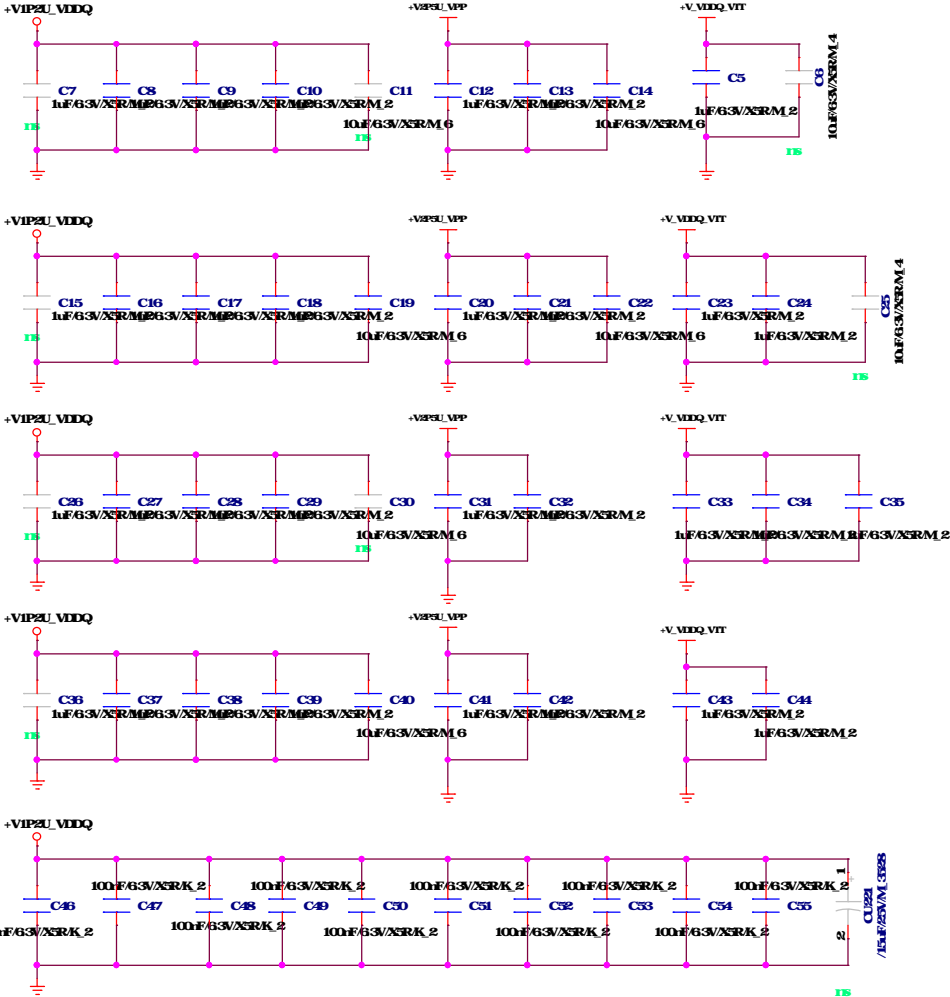
STRAP	FUNCTION	DEFINITION
SPI_CLK		1: USE 48MHZ CRYSTAL CLOCK AND GENERATE BOTH INTERNAL AND EXTERNAL CLOCKS (DEFAULT) 0: USE 100MHZ POE CLOCK AS REFERENCE CLOCK AND GENERATE INTERNAL CLOCKS ONLY
SYS_RST#		1: NORMAL RESET MODE (DEFAULT) 0: SHORT RESET MODE





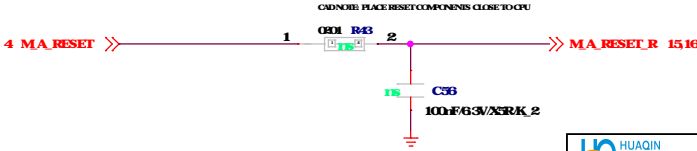
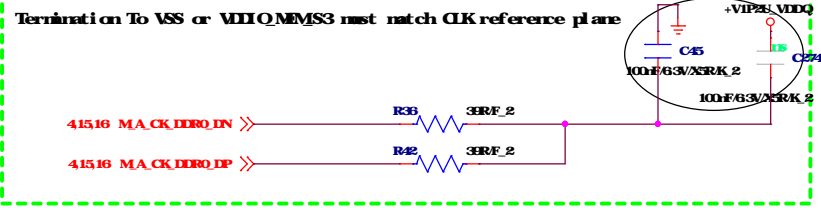
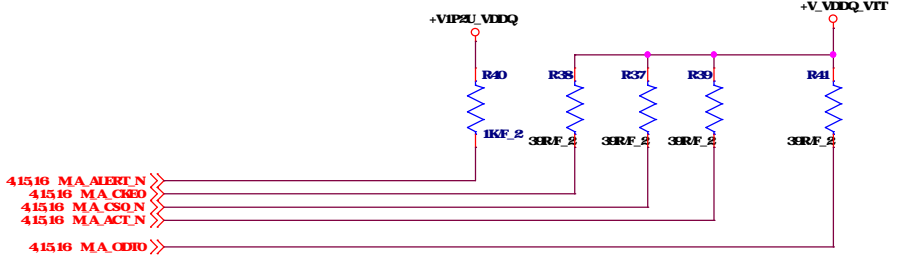
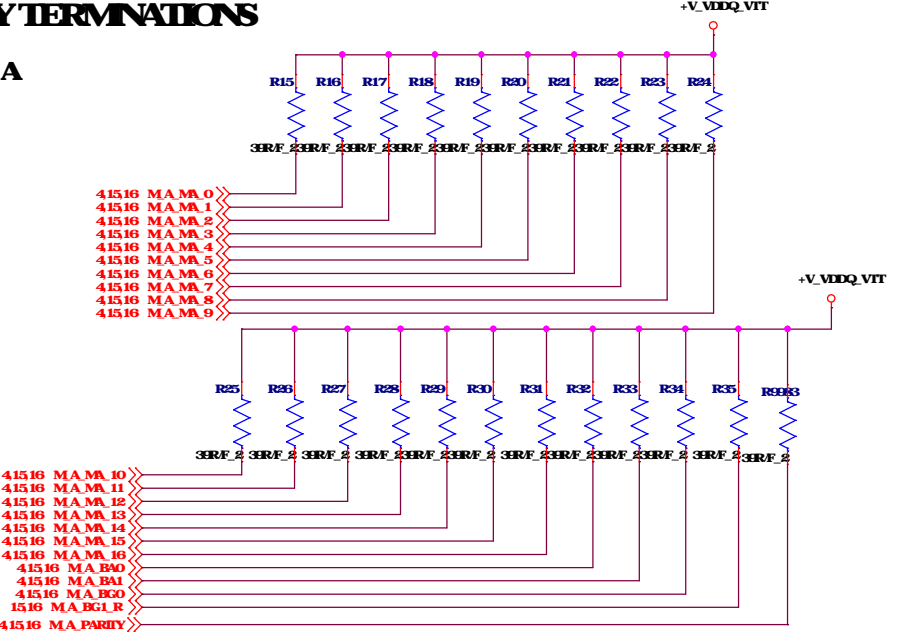



DECOUPLING CAPACITORS FOR DDR CHANNELA

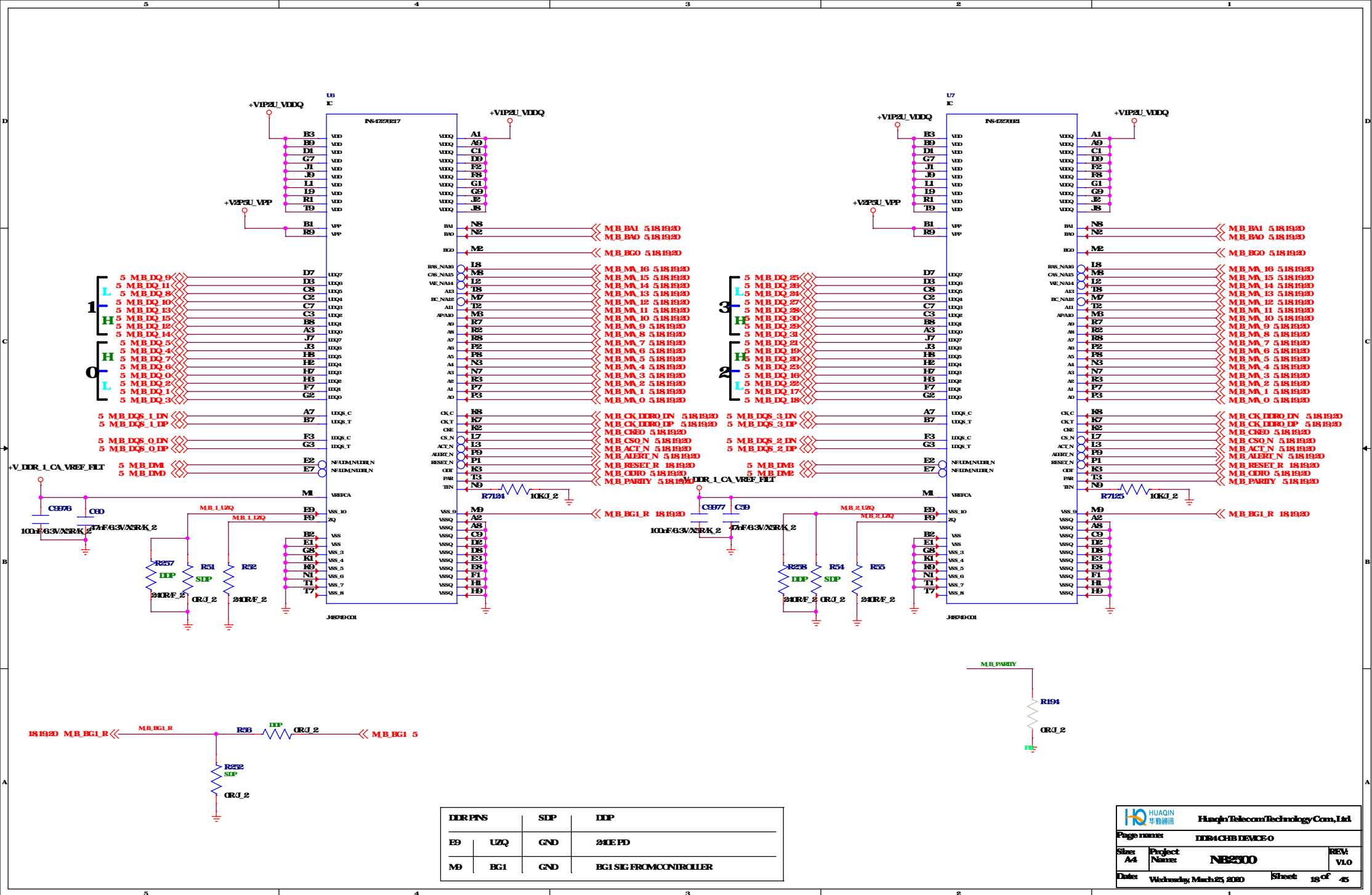


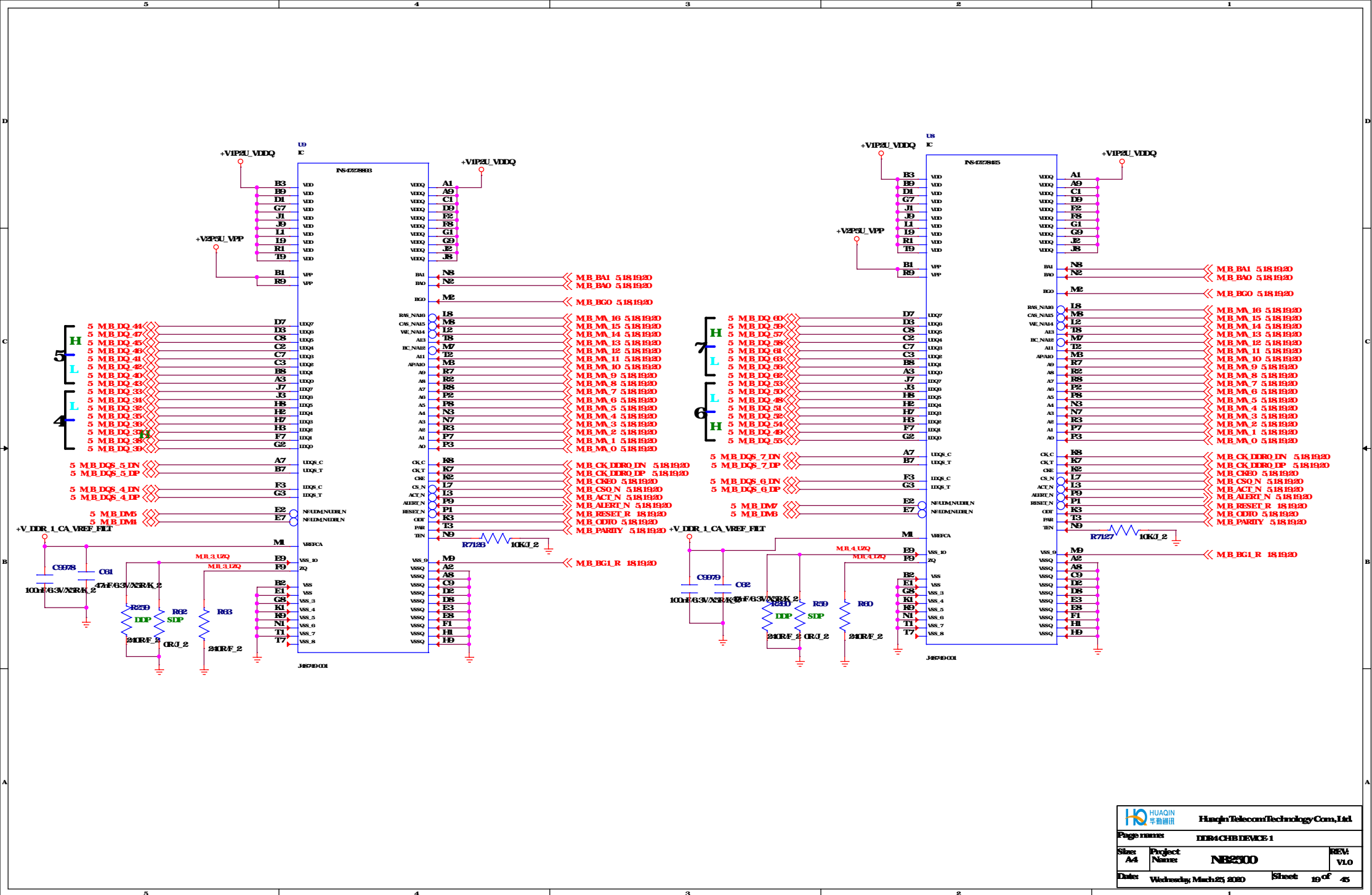
MEMORY TERMINATIONS

CHANNELA

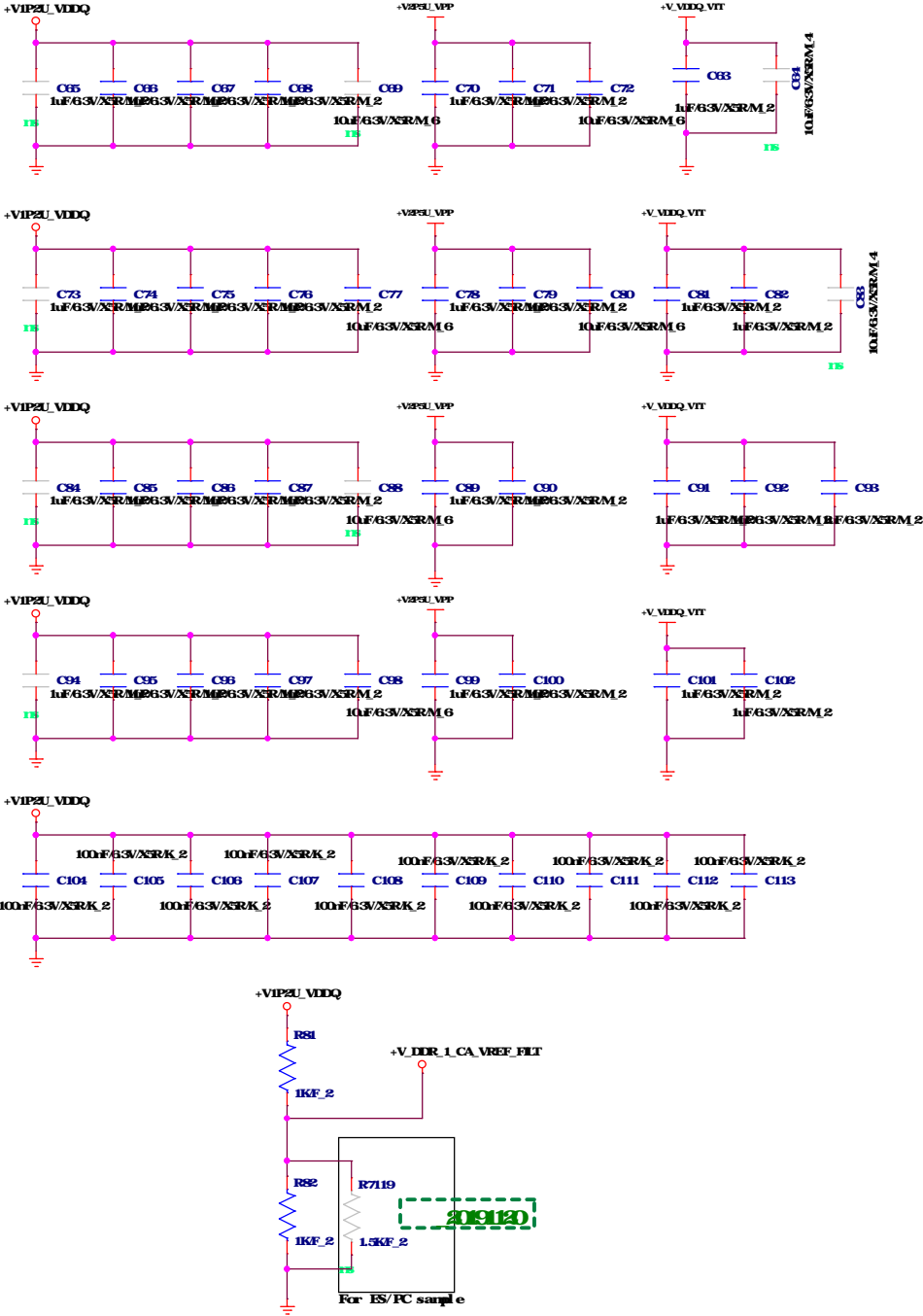


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Page name:		DDR4 CHA CAP&TERM	
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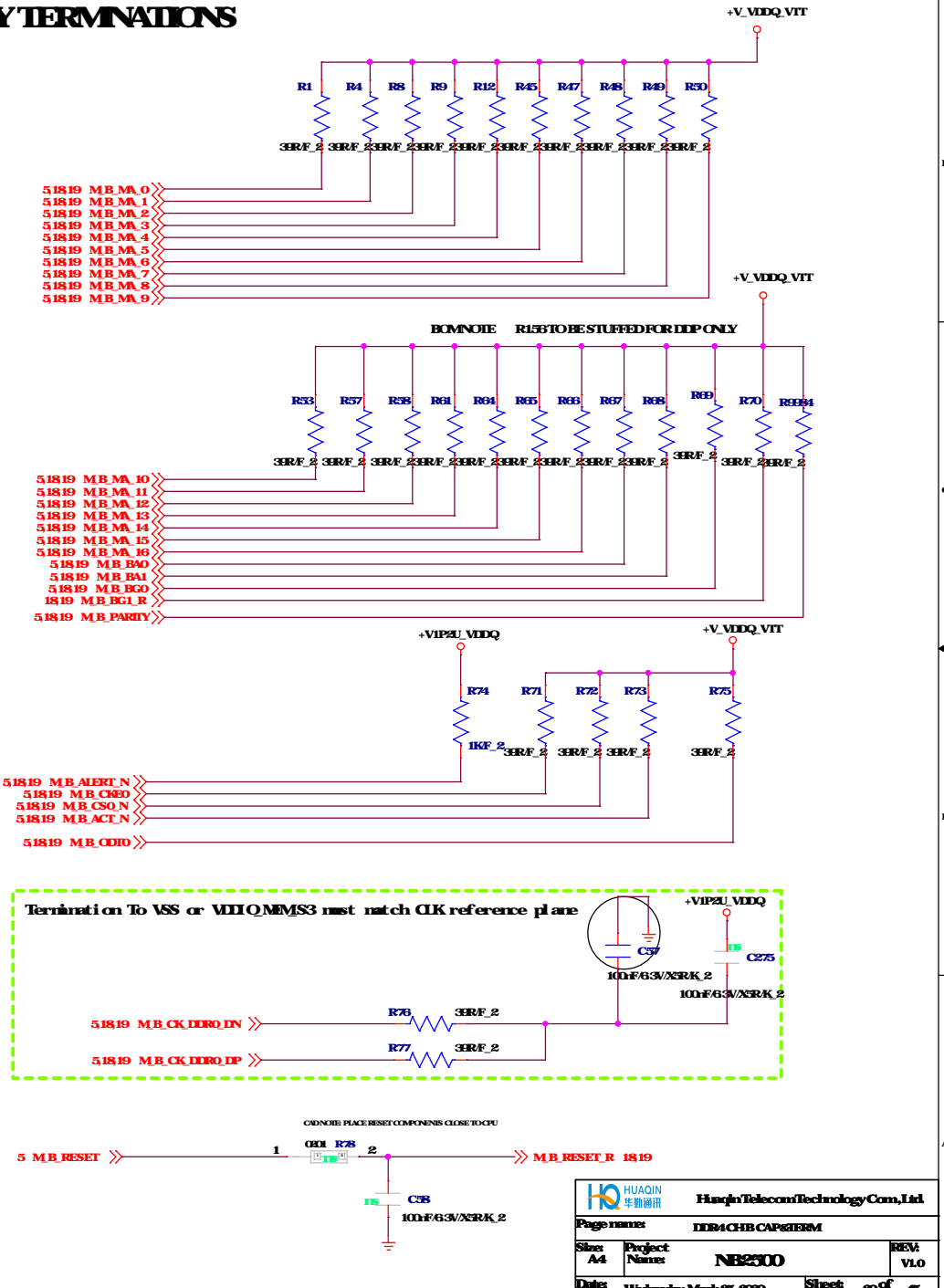


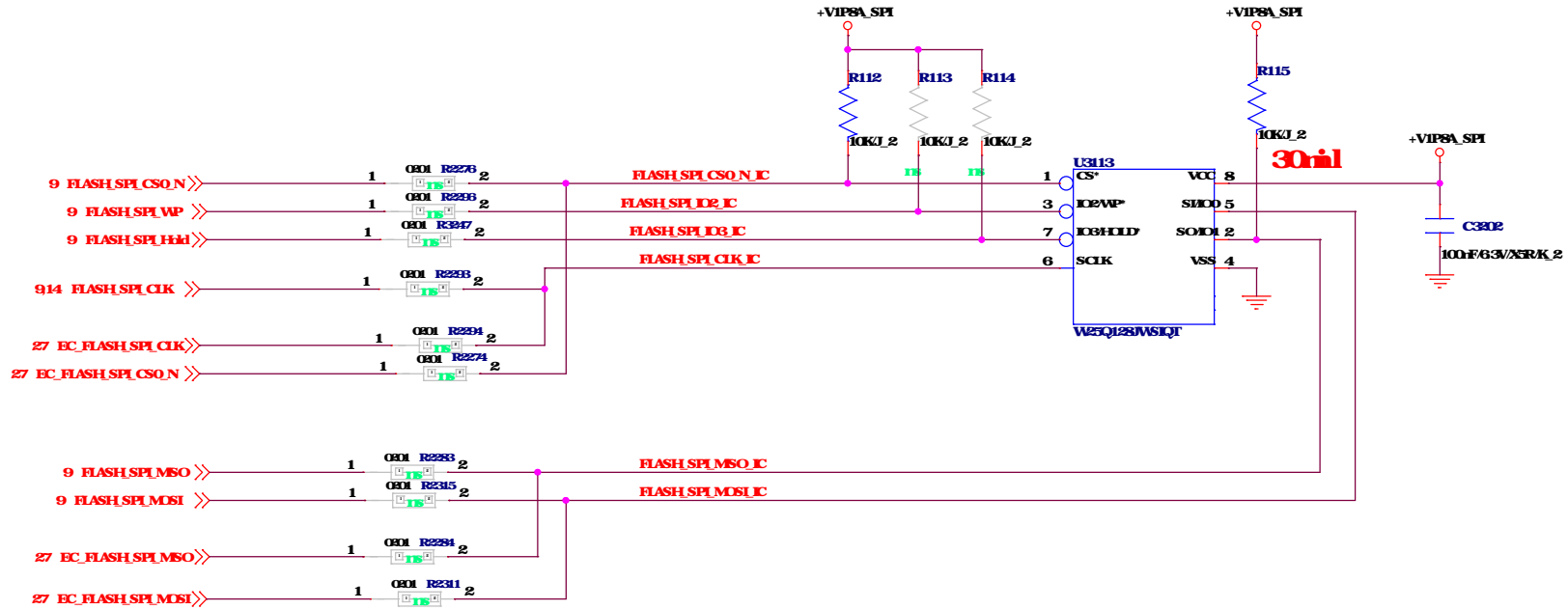
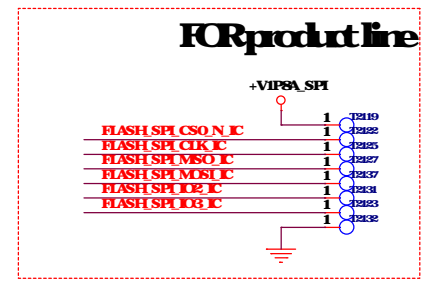
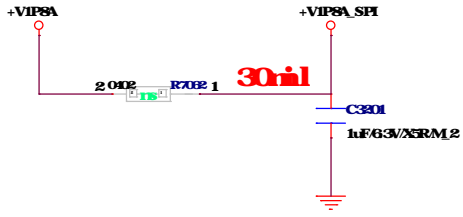


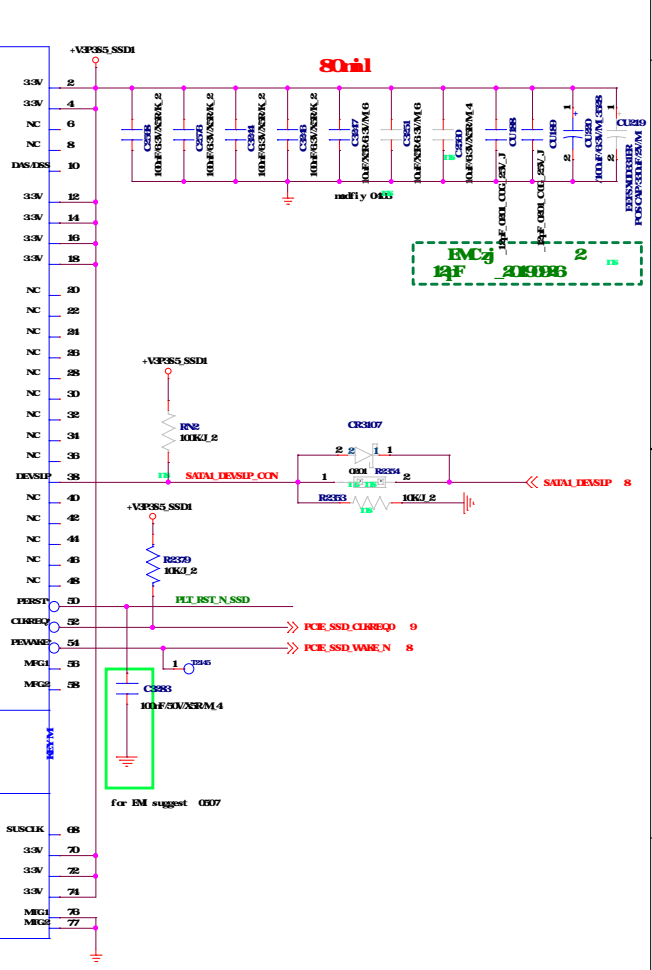
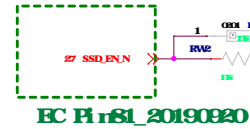
DECOUPLING CAPACITORS FOR DDR CHANNELA



MEMORY TERMINATIONS



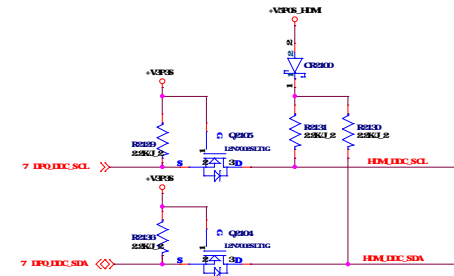
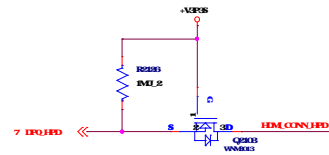
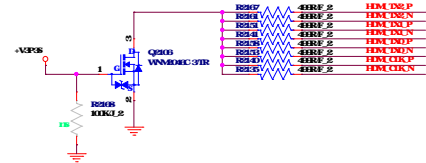
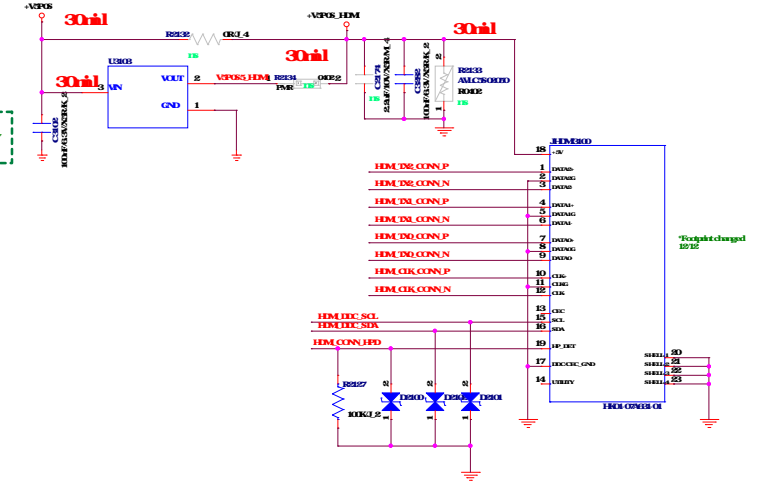
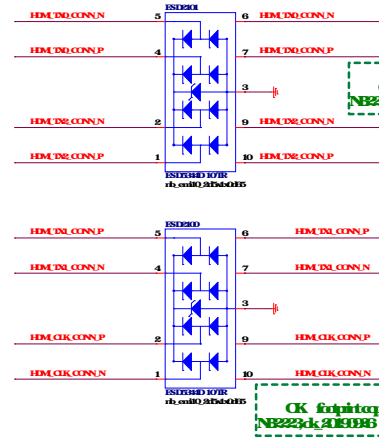
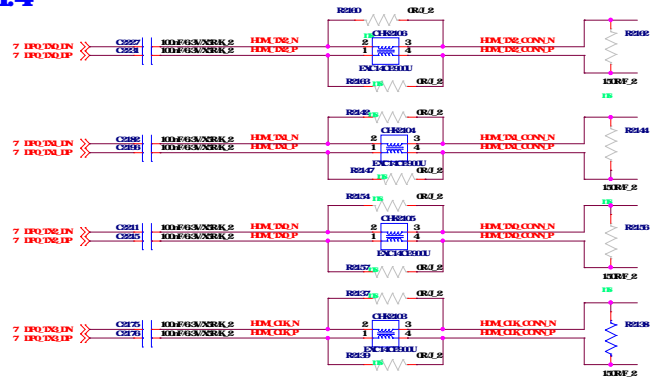







# HDMI4

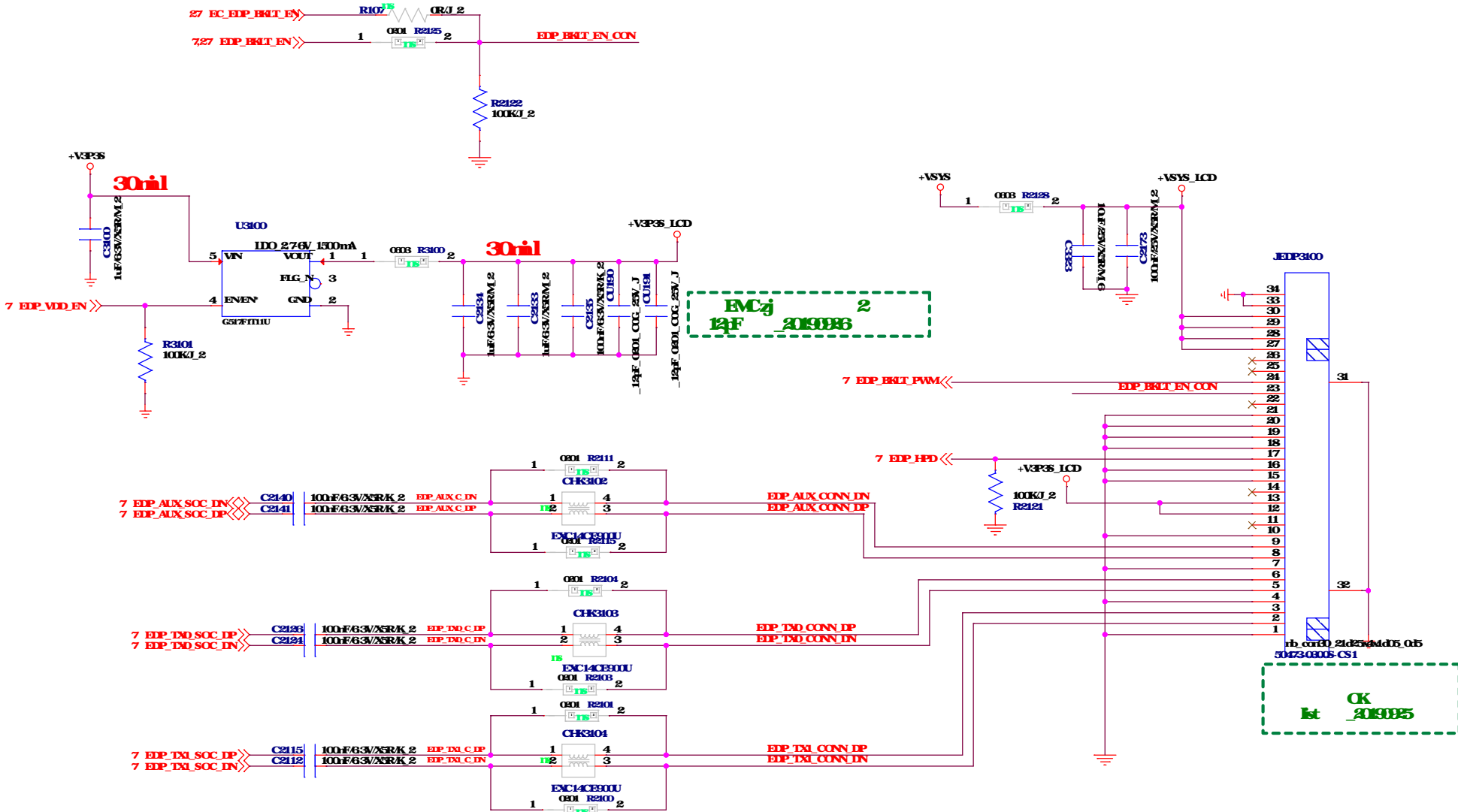
## Signal

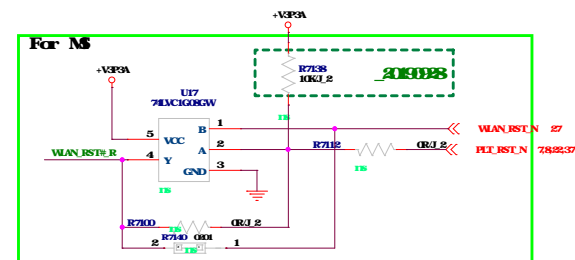
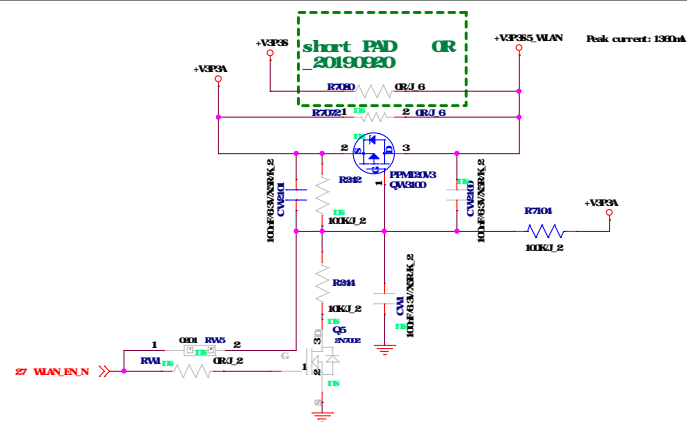


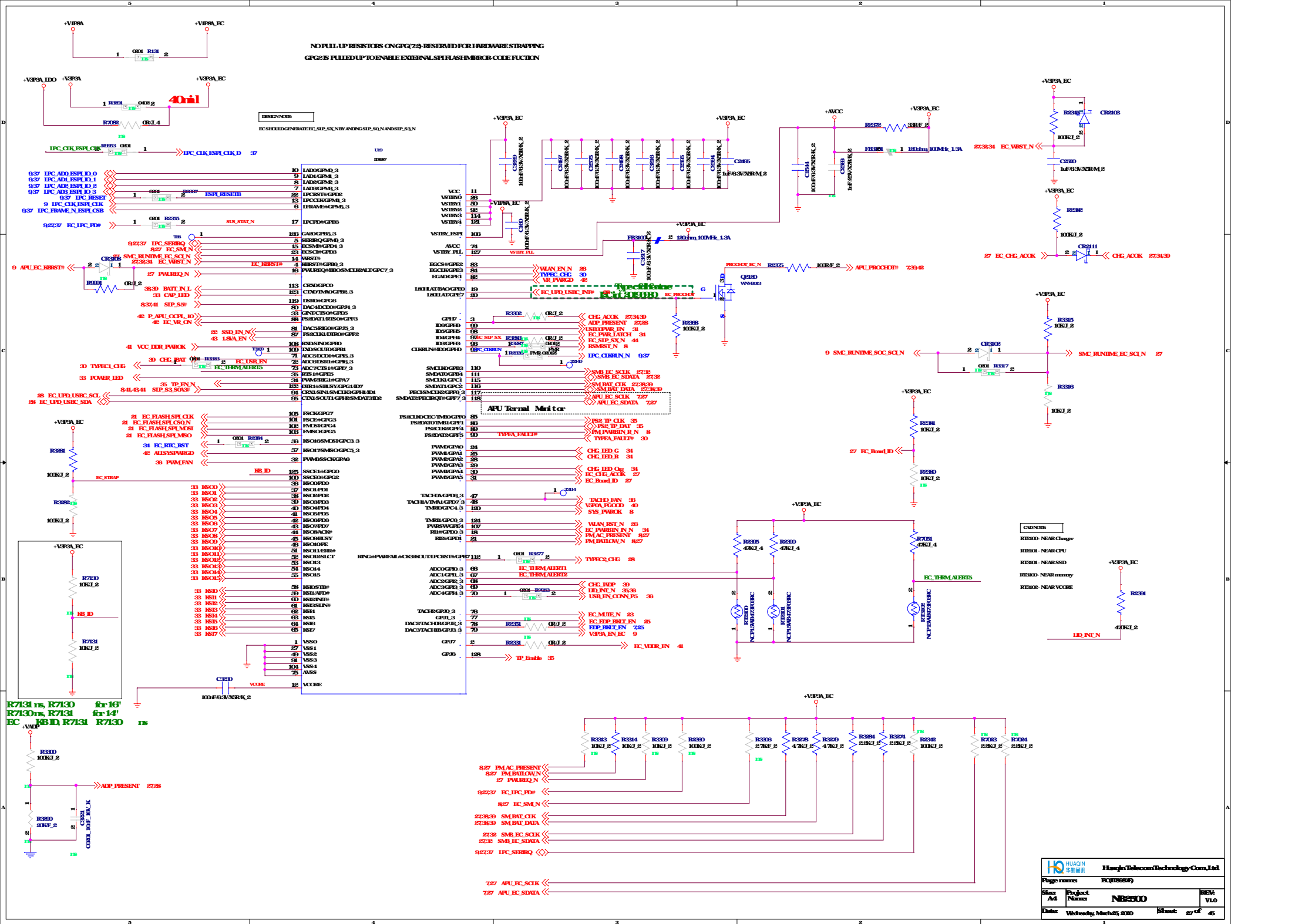
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Page number		HDM	
Size	Project Name	NAME	REV
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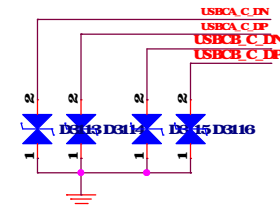
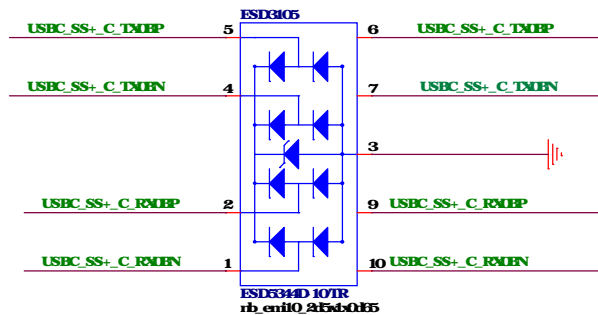
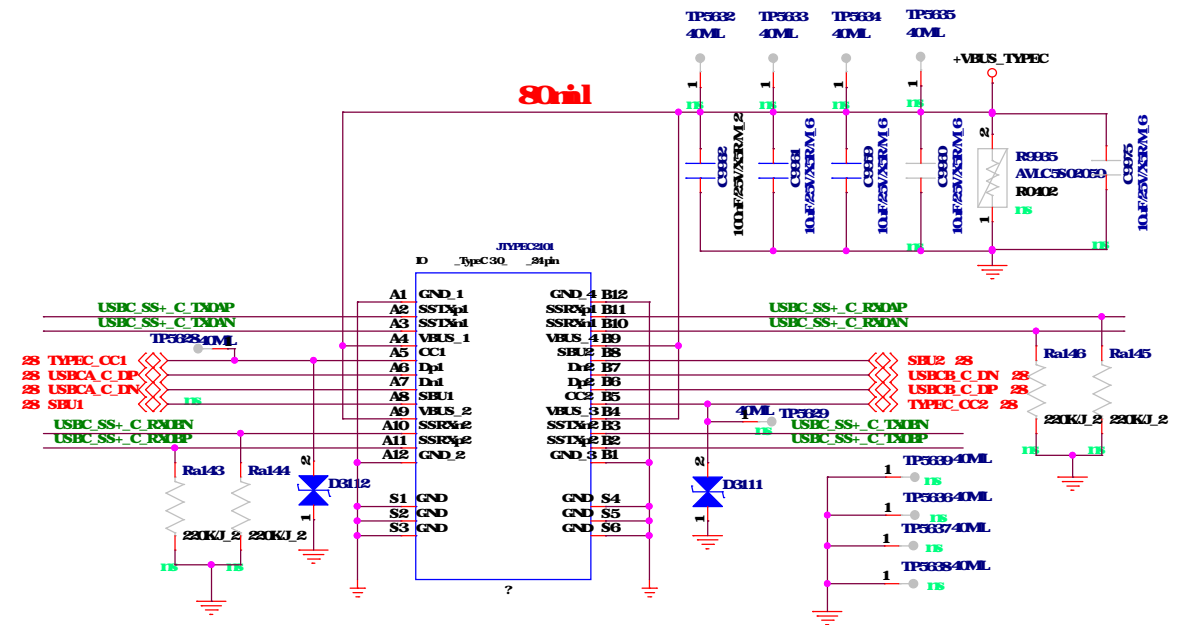
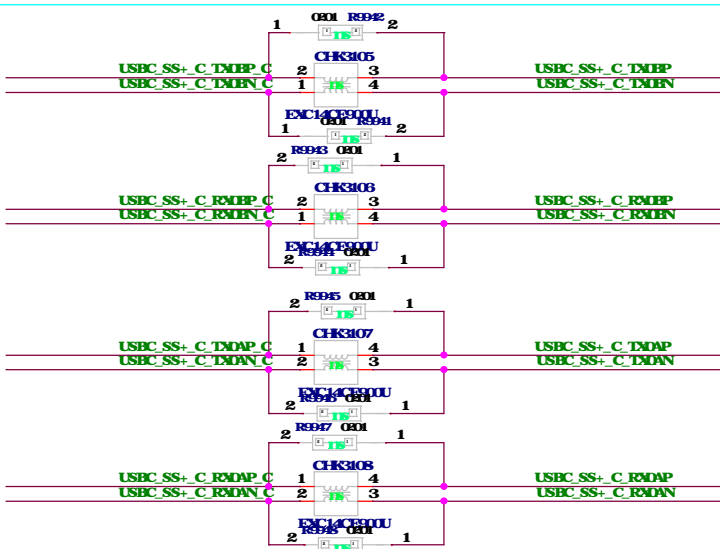
# LCD PANEL

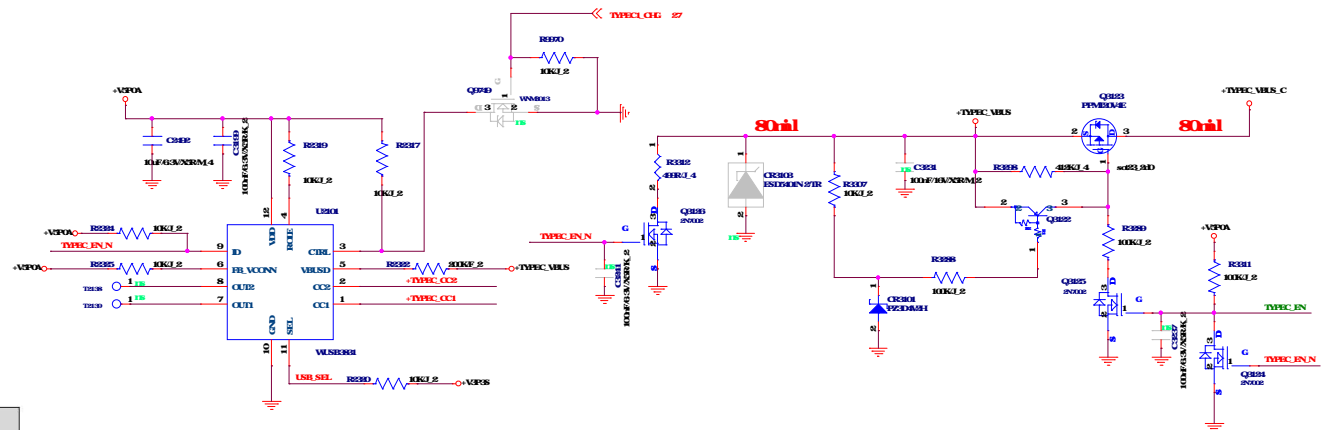




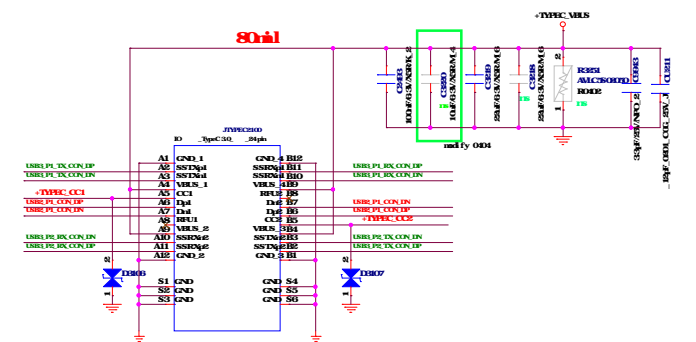
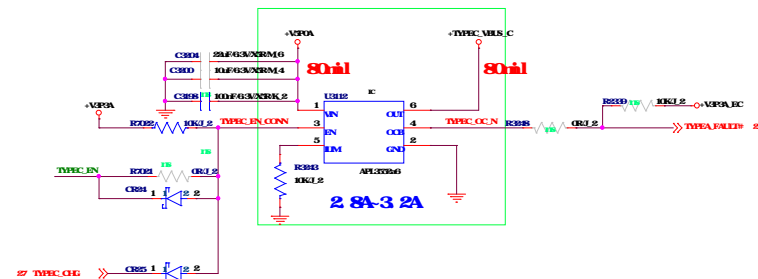
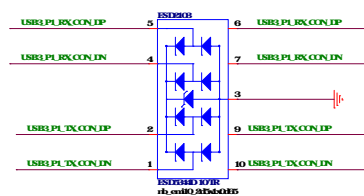
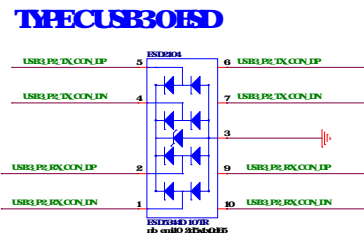






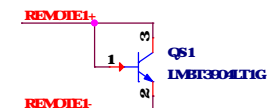


PORT A CHANNEL	PORT B OR PORT C CHANNEL CONNECTED TO PORT A CHANNEL	
	SEL = L	SEL = H
A0p	B0p	C0p
A0n	B0n	C0n
A1p	B1p	C1p
A1n	B1n	C1n

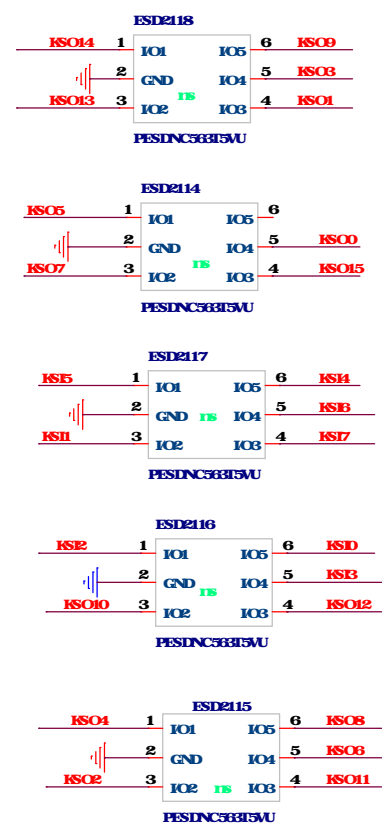
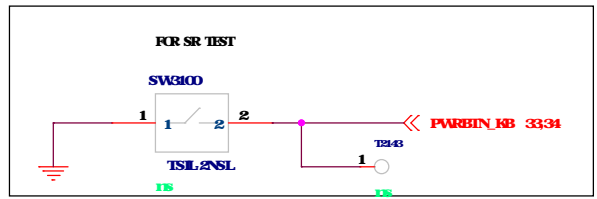
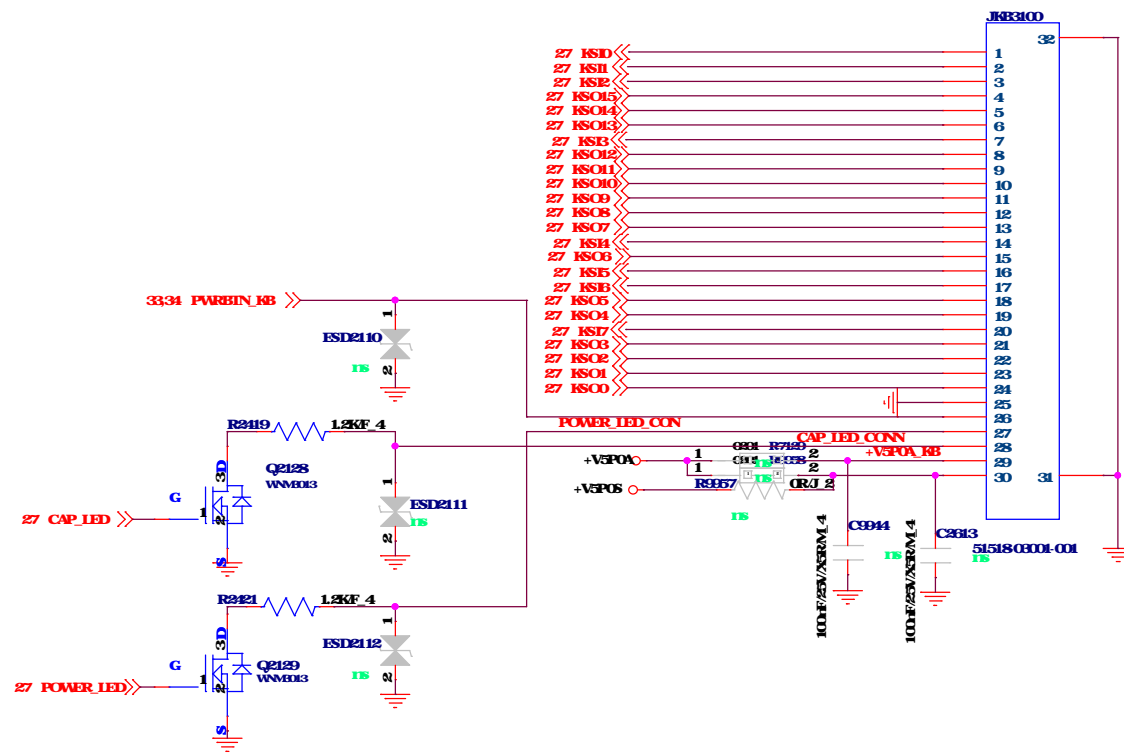




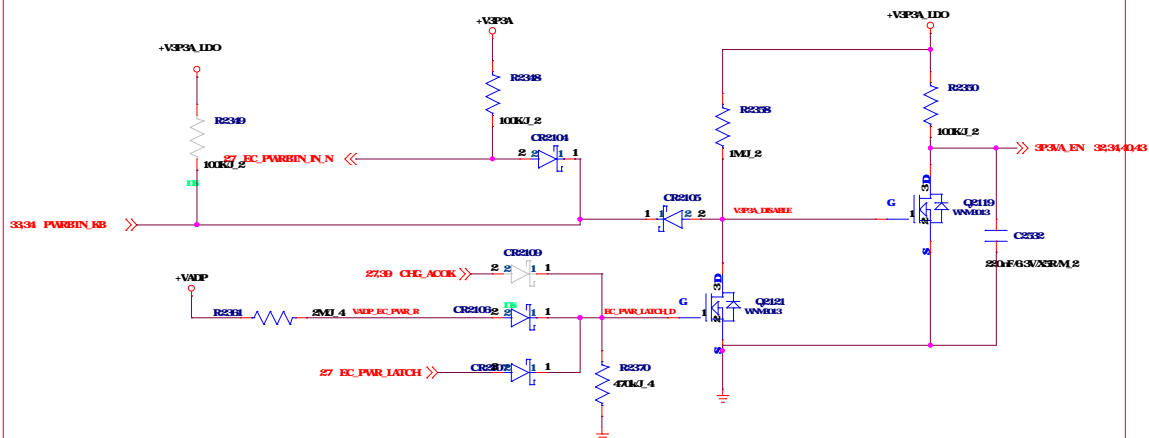
REM01E1+/-, Trace width/space: 10/10 mil, Trace length <8'  
Connect guard traces to GND on either side of the  
DNP DAN traces



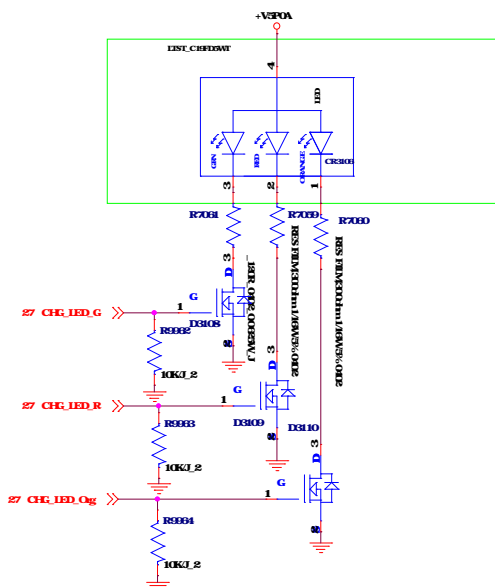
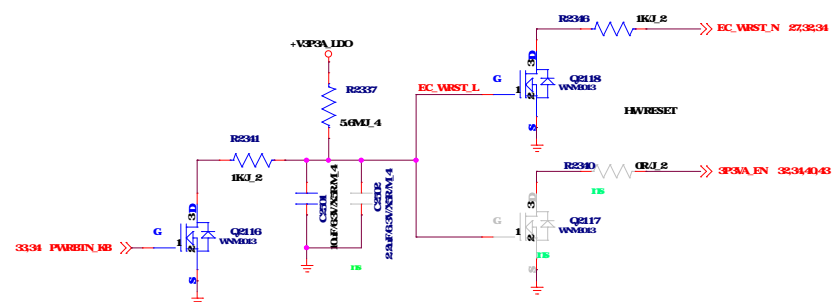




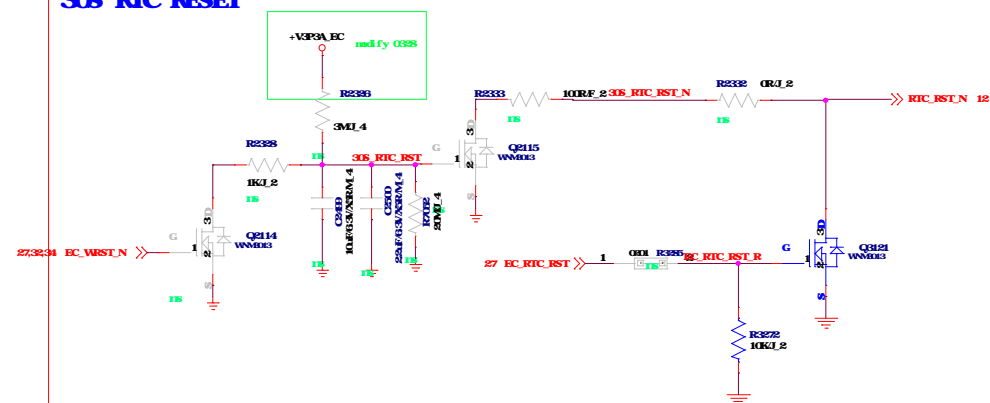
## PVR ON LOGIC

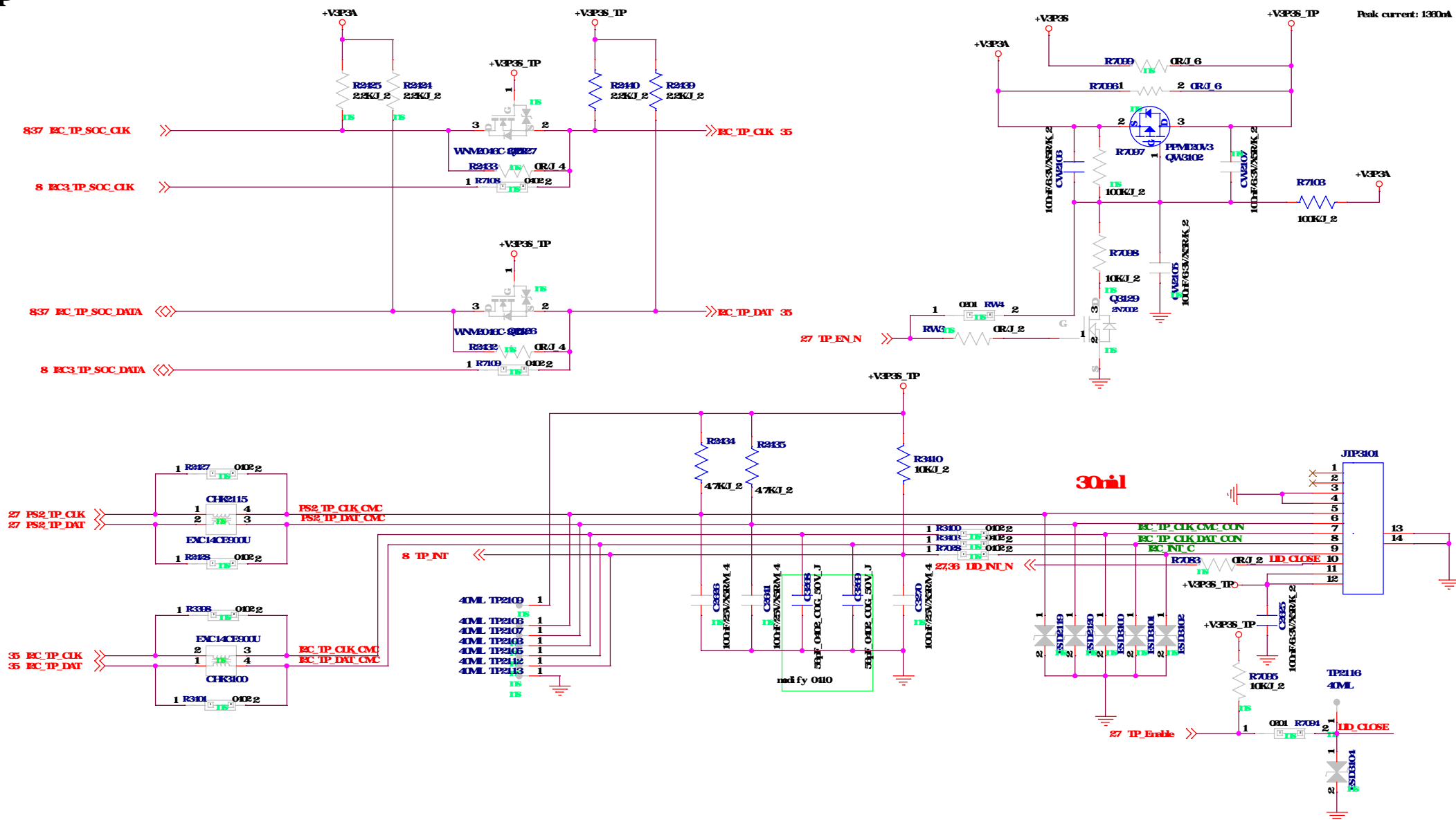


## 158 Force Power Down

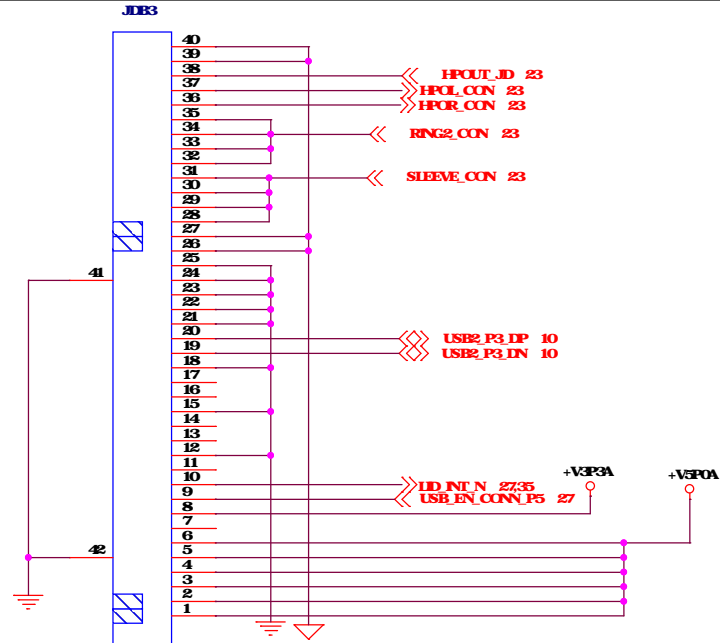


### 30S RIC RESET

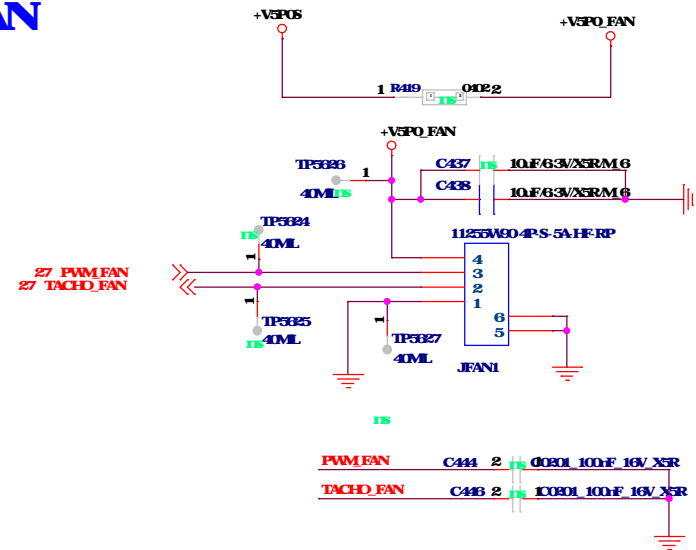




# DB

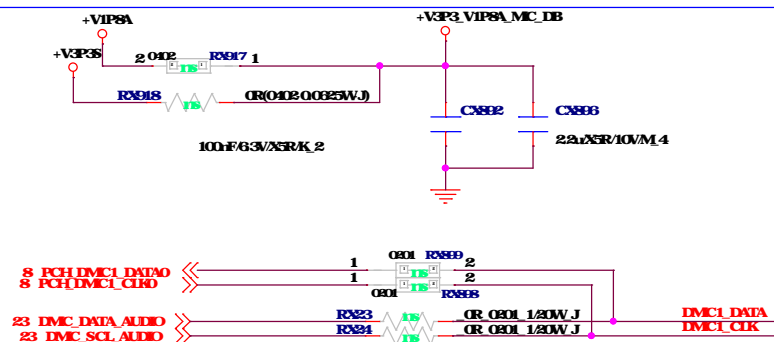


# FAN

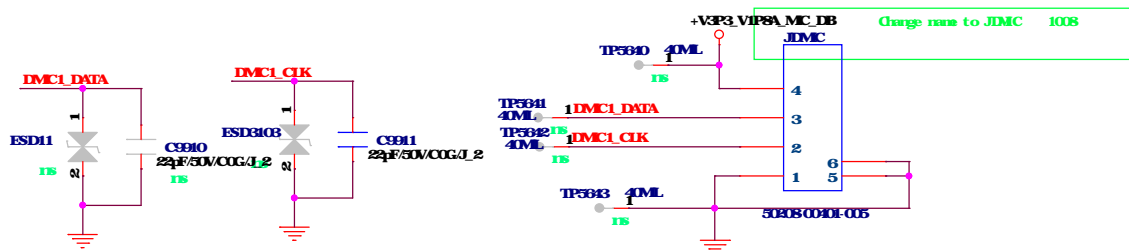
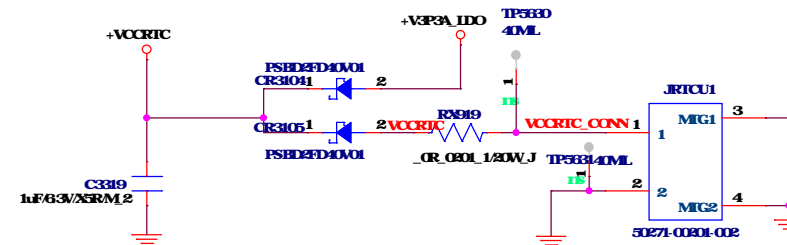


# DMC

rb,cm40 23Bd4Bd5  
ARC34S41P6A1Z



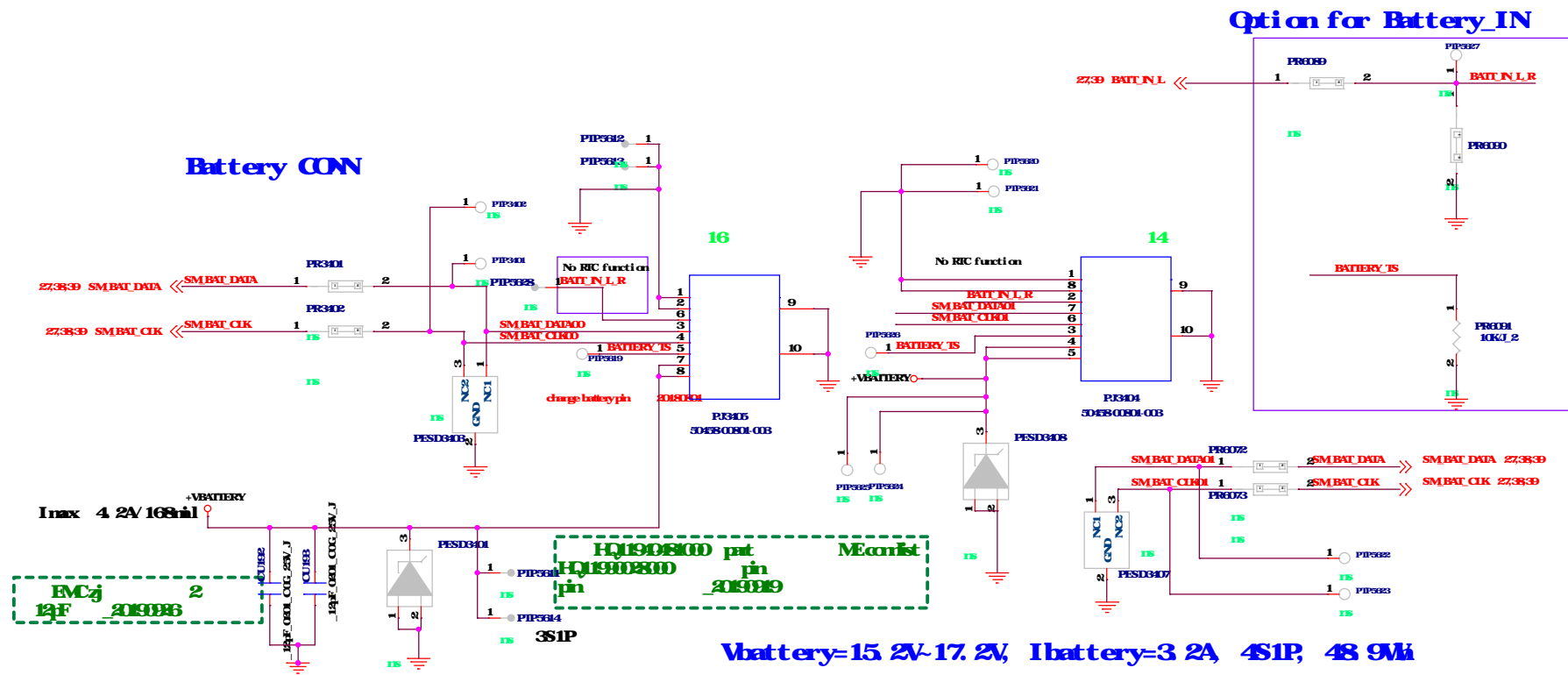
# RTC



HUAQIN 华勤通信		Huaqin Telecom Technology Co., Ltd.	
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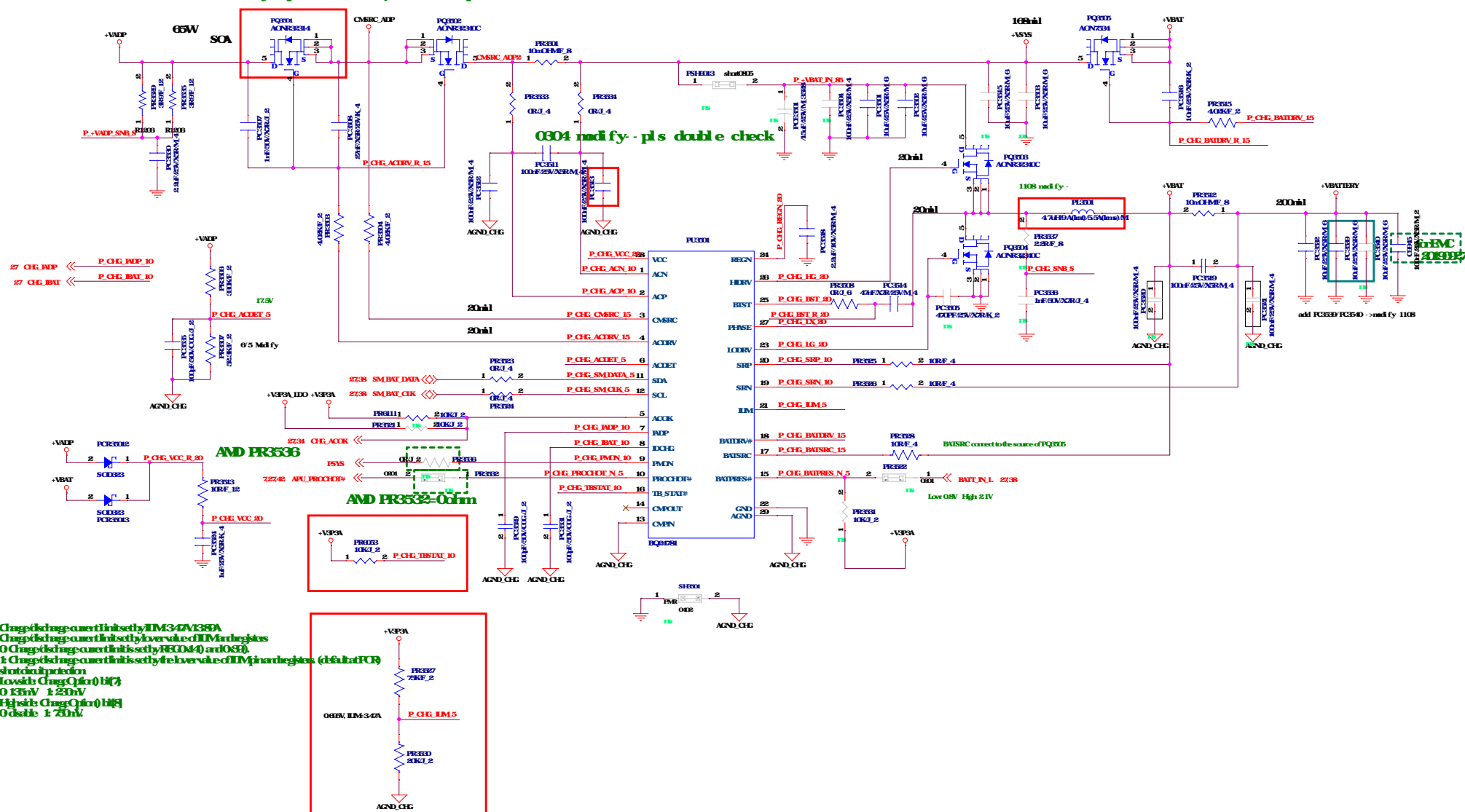


# DCN&BAT CON



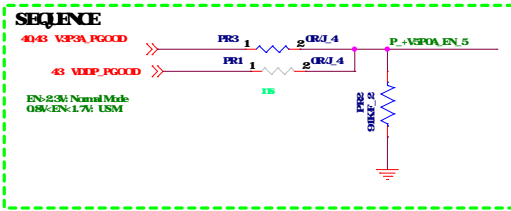
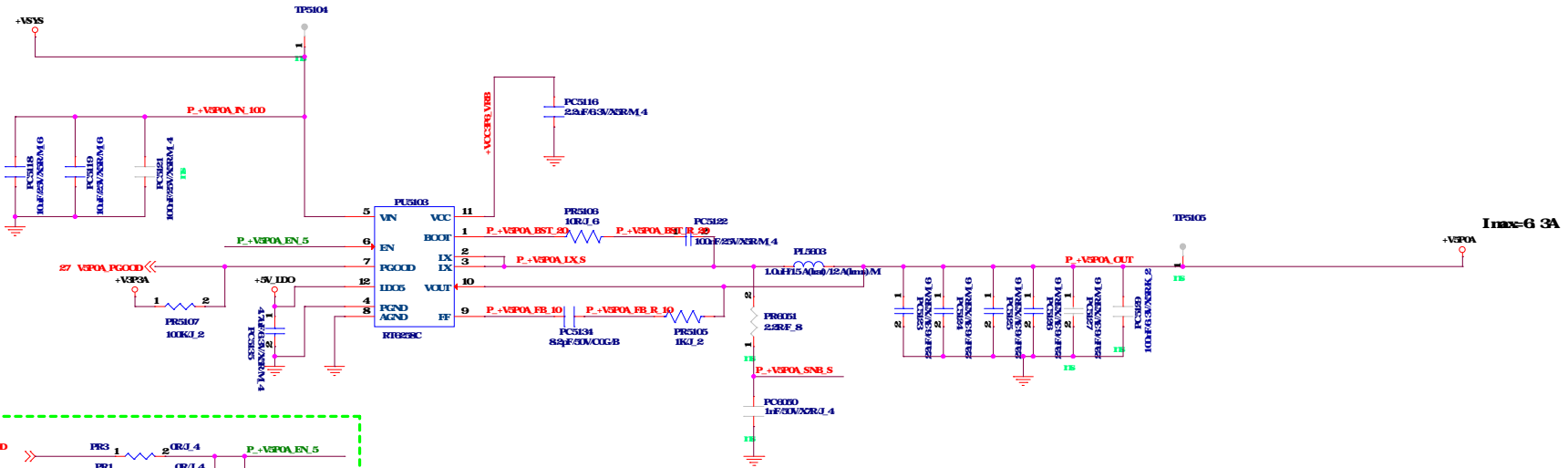
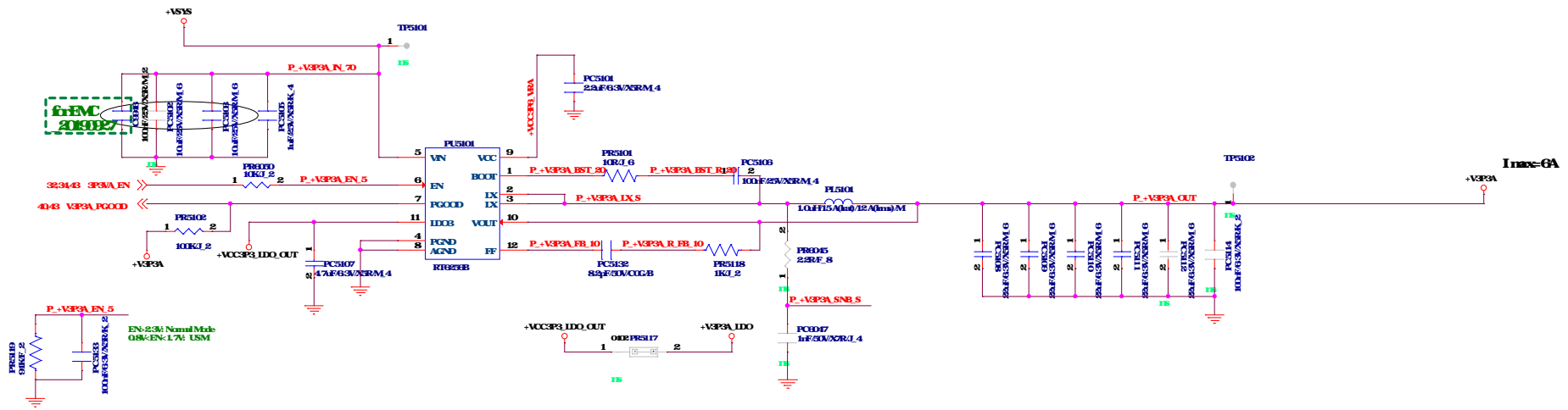
## SystemCharger[BQ24781]

**0225 modify - pls check HQ code&footprint**

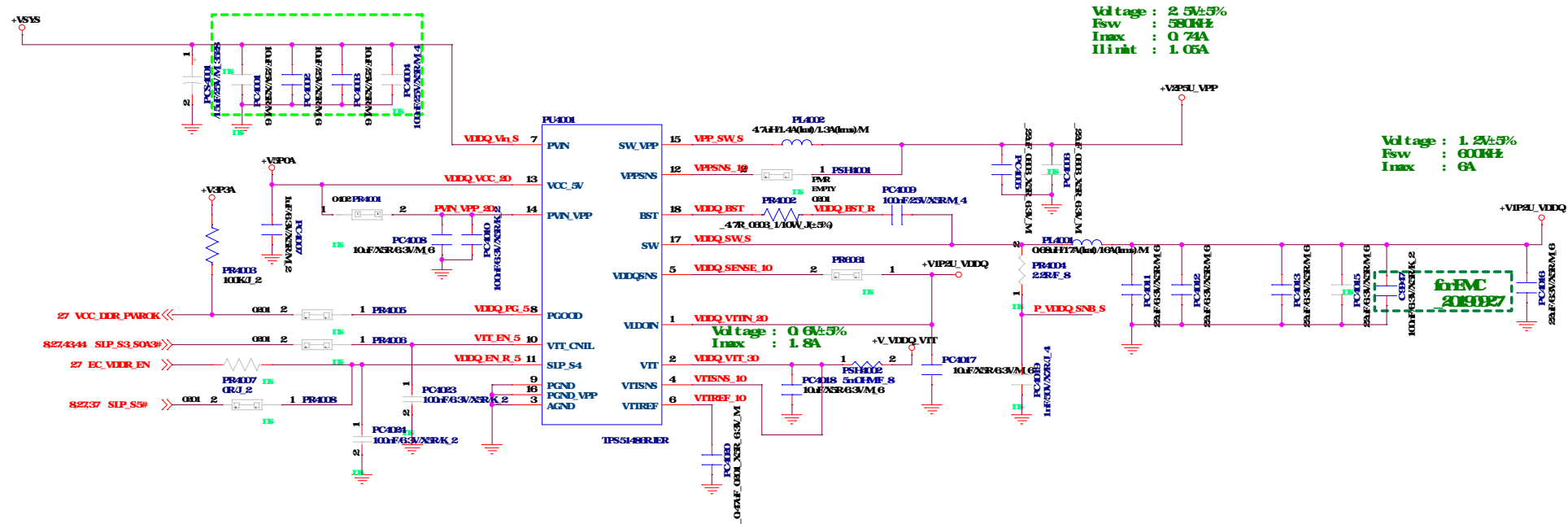


**Note: PR35275k, PR35302K, Lin#347A/1389A**

# +V3P3A+V5P0A[SystemPower]

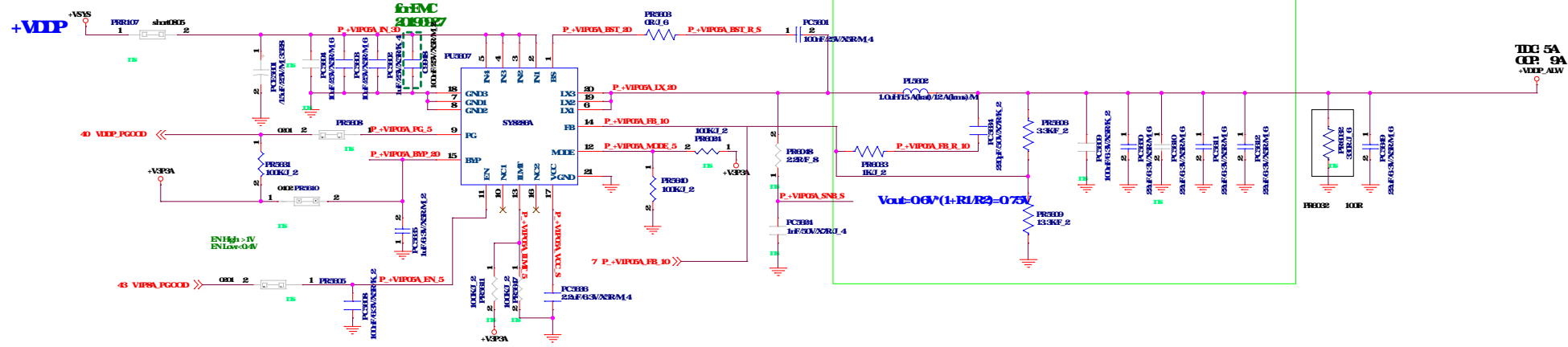




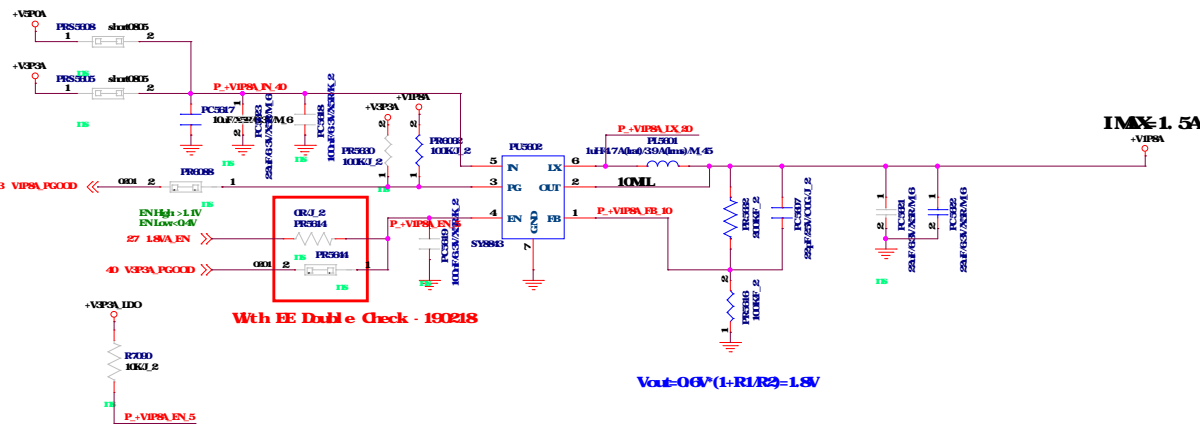




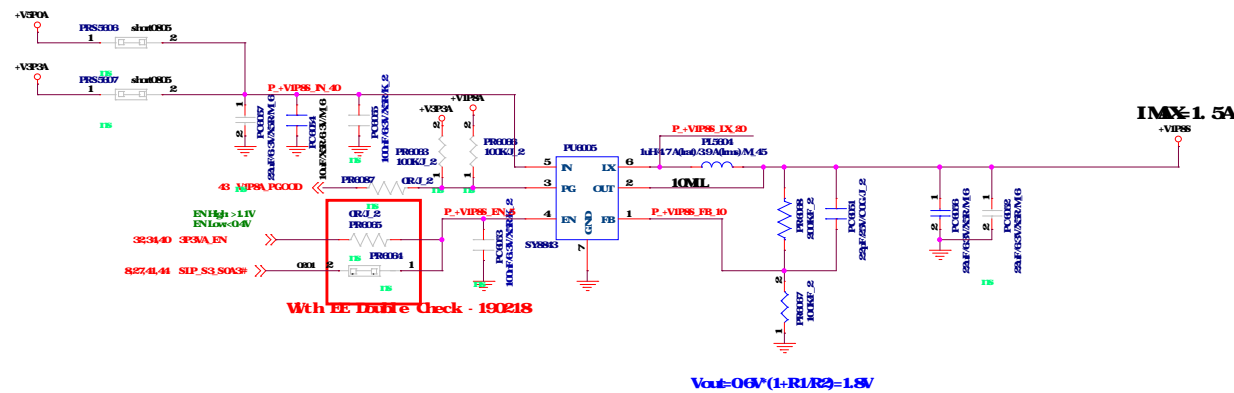
# +VDDP/+VIP8A



IMT pinfloating I<sub>lim,min</sub>=93A



With EE Double Check - 190218

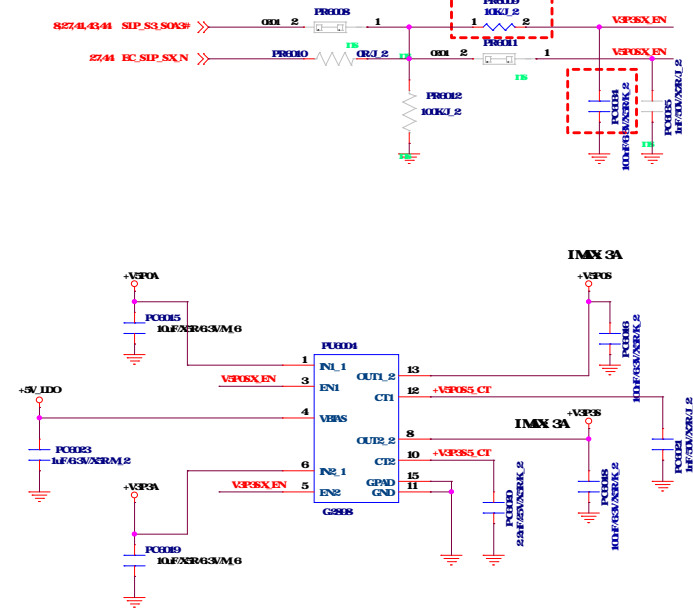


With EE Double Check - 190218

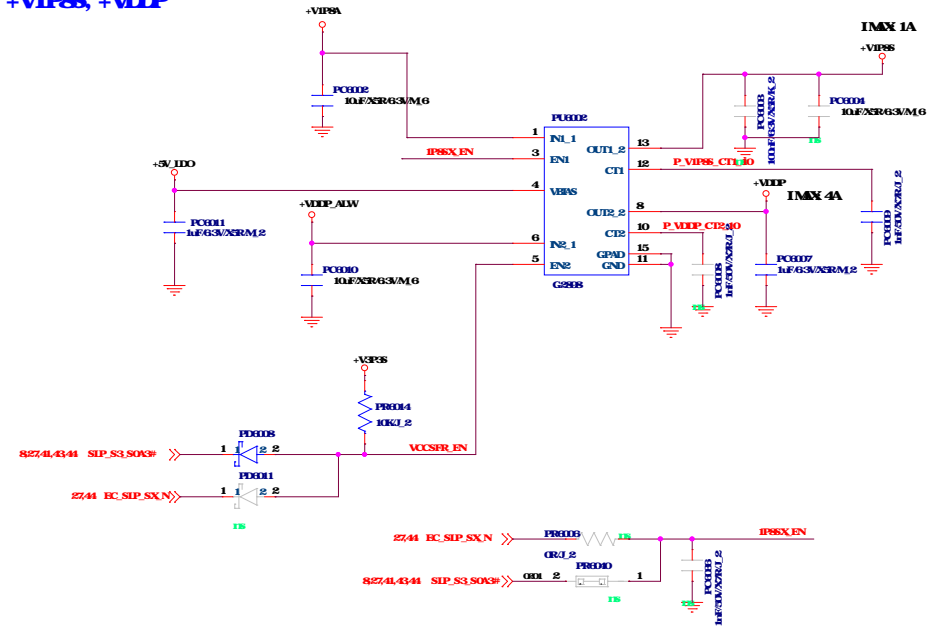
# PWR\_Load switch

+V3P3S, +V5P0S

0305 Modify for EE timing



+VIP8S, +VDP



FOR EMC

FOR EMC

